Agilent’s DisplayPort Solutions
Presentation Agenda

- Introduction to DisplayPort
- DisplayPort Technology
- Compliance Testing in DisplayPort
- Measurement Tasks in DisplayPort
- Agilent Engagement
- Solutions for DisplayPort
- Test Drive the U7232A Source Compliance Test Software
Introduction to DisplayPort

DisplayPort Bio:

- Started out as the ‘Greenland Project’ by Intel, Dell Genesis, and Tyco
- Now Under the Administration of VESA
- Version 1.0 created May 2006
- Version 1.1 March 2007
- Version 1.1a January 2008
- Replacement Digital Transport Interface for DVI
- Pushed by Dell, HP, Intel
- Incorporates HDCP (High Definition Content Protection)
# Introduction to DisplayPort

Some VESA Companies…

VESA ~ 170 Members

<table>
<thead>
<tr>
<th>Analog Devices</th>
<th>Genesis Microchip</th>
<th>Allion</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parade</td>
<td>Luxtera</td>
<td>Mitsibushi</td>
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<td>AMD</td>
<td>Semtech</td>
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<td>Dell</td>
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<td>Kotura</td>
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<td>Vativ Technologies</td>
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<td>Tyco</td>
<td>IBM</td>
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<tr>
<td>Hosiden</td>
<td>Broadcom</td>
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<tr>
<td>Molex</td>
<td>Conexant</td>
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<tr>
<td>Texas Instruments</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

High degree of overlap into HDMI.org
DisplayPort Applications

- Computer Graphics Controller
- Computer Display
- Multimedia monitor
- Device concentrator
- Device replicator
- Repeater
- Display controller
- Multimedia / AV selector (e.g. Home theater receiver)
- Legacy converter / Protocol Bridge (e.g. DP <-> HDMI/VGA/DVI)
- Handheld Video
- Chip-chip communications
- Cables
DisplayPort Principal Use
Introduction to DisplayPort

Where it Fits...

SATA, SCSI, FibreChannel, DDR, FBD, PCI Express, GbE, USB
Introduction to DisplayPort
What does it mean?

- Fewer Connectors
- Fewer ICs

- Cheaper
- Less Power
- More Available Pins
- Has Headroom

No Wonder Dell/HP is pursuing this!
They engaged with DisplayPort as part of corporate strategy... The first time they have pushed and led a new standard
DisplayPort Technology Overview

1-4 high speed lanes (1.62, 2.7Gb/s) – Source to Sink only
- Fixed data rate independent of display refresh
Auxiliary channel for bidirectional link communication (1Mb/s)
Auto detect of cable plug/unplug
Scalable to DDR/QDR rates for higher capacity displays
DisplayPort Technology (Main Link Lanes)

Silicon:
• Structure leveraged from PCI Express
• Implementable on 65nm process
• Termination Voltage must be <2volts (internal to IC)

Receiver
• PLL BW=10MHz effective

Data Rate
• 1.62 Gbs
• 2.7 Gbs (units supporting 2.7 must support 1.62 as well)
DisplayPort Technology (Main Link Lanes)

Lanes

- Each lane is Differential, 100Ω.
- 1, 2, 4 lane models for video data transport. 4 lane model capable must support 1 & 2 lane models. 2 lane model must support 1 lane model. Lanes are uni-directional
- ANSI standard 8b/10b
- Each lane has separate clock recovery
- Single ended lines of each lane are source and sink terminated and biased. No external pull-up is needed for test equipment.
**DisplayPort Technology (Main Link Lanes)**

**DisplayPort Signal Parametrics**

- 400, 600, 800, 1200 mVolts pk-pk. 1200 is optional
- 0, 3.5, 6, 9.5 dB pre-emphasis. 9.5dB is optional
- No combination of voltage and pre-emphasis can exceed 1200mVolts pk-pk
- Spread Spectrum Clocking (30-33KHz spreading frequency, downspread)
- Rise time not to be below 75ps
- Total Jitter and Non-ISI jitter is specified
DisplayPort Technology (Aux Channel)

- Designated Control Link lane called ‘the AUX Channel’ specified. Operates at 1Mbs and is used in Link Training and Link Management and is Bidirectional Half Duplex

- The Transmitter is the master
- Receiver gains attention by pulling down on the Hot Plug Detect Line
- Manchester II coding
<table>
<thead>
<tr>
<th></th>
<th>HDMI</th>
<th>DisplayPort</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Market</strong></td>
<td>HDTV/Gaming</td>
<td>PCs</td>
</tr>
<tr>
<td><strong>Technology</strong></td>
<td>TMDS (8B/10B)</td>
<td>PCI-Express/New (8B/10B)</td>
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<tr>
<td><strong>Configuration</strong></td>
<td>4 lanes (3 Data, 1 Ck) Differential, DC coupled</td>
<td>1, 2, or 4 lanes (Embedded Clock) Differential, AC coupled</td>
</tr>
<tr>
<td><strong>Bit Rate</strong></td>
<td>250Mbs to 3.4Gbs per lane</td>
<td>1.62 or 2.7Gbs</td>
</tr>
<tr>
<td><strong>Tx/Rx Negotiation</strong></td>
<td>EDID/DDC</td>
<td>Aux Channel</td>
</tr>
<tr>
<td><strong>Compliance</strong></td>
<td>Authorized Test Centers</td>
<td>Qualified Test Houses</td>
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<tr>
<td><strong>Ownership</strong></td>
<td>HDMI.org</td>
<td>VESA</td>
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<td><strong>Std/Royalty</strong></td>
<td>Closed/Yes</td>
<td>Open/No</td>
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<tr>
<td><strong>Driving Need</strong></td>
<td>HDTV and HDCP</td>
<td>Margin</td>
</tr>
<tr>
<td><strong>Models</strong></td>
<td>External</td>
<td>External and Embedded</td>
</tr>
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</table>
## DisplayPort Compliance

A lot like USB…

<table>
<thead>
<tr>
<th>Plugfests</th>
<th>Focus to facilitate interoperability by exposure and by test</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logo</td>
<td>Yes</td>
</tr>
<tr>
<td>Certification</td>
<td>VESA approved independent Test centers: Allion, ETC, NTS, Contech Research</td>
</tr>
<tr>
<td>Product Change Criteria</td>
<td>Re-certification required at Test House if Critical or Significant changes are made</td>
</tr>
<tr>
<td>Self Certification</td>
<td>Not yet, but work is proceeding on this</td>
</tr>
</tbody>
</table>

Compliance maturity obviously is low at this point:

- **VTM will administer the compliance testing at Plugtests.**
- **No official statement on interoperability test regimen like USB**
- **VTM is driving ‘conscious interoperability’ over time by compliance test, plugfest test and interoperability tests. The program starts ‘loose’ and gets more rigorous over time**
DisplayPort Compliance (Official Compliance Process)

DisplayPort Compliance Checklists

- Link Layer CTS
  - Test 1
  - Test 2
  - Test 3

- Phy Layer CTS
  - Test 1
  - Test 2
  - Test 3

VESAS approved Test Center

Customer

Product

Customer

DisplayPort Logo License Agreement

Logo Granted

Compliant Product List

DisplayPort Validation Tasks (Phy/Link)

Source (TX) Channel Test

- High speed lanes
  - Link training
  - Tx mask compliance (noise, jitter)
  - Pre-emphasis/Non-pre-emphasis
  - Skew
- Aux Channel
  - Link negotiation and training
  - Sink device (EDID) support
  - Error injection
- Hot Plug
- SSC support
- Tx <-> Source connector interconnect
- Multimedia (audio, video, sink event)

Link Layer Test

- Source reference
- Sink reference
- Branch test (coordinated source/sink)

Sink (Rx) Test

- High speed lanes
  - Link training
  - Jitter/noise tolerance
- Aux Channel control
- Hot Plug
- Link Training, Deskew
- Multimedia (audio, video, source event)

HDCP

- Challenge / response protocol

Branch / Replicator / Concentrator / Bridge Device Test

- Tx/Rx test
- Error handling
- Conversion to proprietary protocol
- BER (with and without interconnect)
- Pre-emphasis repeating
- DP/HDMI/DVI Adapter

Cable / Connector test

- Loss, NEXT, FEXT, Skew, Return loss
Agilent Strategic Intent for DisplayPort

“We will provide comprehensive design validation and compliance test support that makes Agilent the essential partner for enabling deployment of Display Port product”
Agilent DisplayPort Standards Activities

• VESA Member
• VESA Board Member
• Editor of DisplayPort Compliance Test Specification
• Participant in private and public plugfests
• Active collaboration with lead DisplayPort architects
## Agilent Validation Support Model

### Design Simulation
- Link to Model Database
- Devices & Interconnect Characterization

### Device and Board
- Prototype Characterization & Validation
- Bring-Up Test

### System
- System Integration & Functional Validation

#### Physical Layer
- Passive Interconnect Measurements
  - Impedance, Crosstalk, ...
- Device Characterization & Modeling Services
- Physical Layer Test System
  - ADS
  - SPICE/IBIS
  - 86100C with TDR
  - PNA Series VNA

#### Link Layer
- Active Live Signal Measurements
  - Voltage, Jitter, BER, Timing, Packets, ...
- N5990A Test Automation Software Platform
- Serial/Parallel BERT
- 81133/4 Pulse Generator
- 16900 Series Logic Analysis System & Soft Touch Probes
- Protocol Analyzer/Exercisers
- 86100C 50Ghz Infiniium DCA-J Sampling Scope
- DSO80000 /90000 Infiniium Real Time Scopes
- Infinimax Probing System
- Intelligent Parametric Test/Probing Fixtures

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**Agilent Technologies**

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Familiar Measurement and Development Problems

Phy Layer Test Points

Content → Video Transmitter → Media → Video Receiver → Display

Link Layer/Protocol Test and Control Points
DisplayPort Support Overview

Compliance Test

Test fixtures and probes

– Plug (Source, Sink, Link layer)
– Receptacle (BIT-DP-RTF-0001)

• Transmitter test
  – Physical Layer (Scope)
  – Link Layer (Reference Sink)

• Receiver test
  – Physical Layer (Bert)
  – Link Layer (Reference Source)

• Cable/Connector/Interconnect test
  – TDR / VNA
Validation and Compliance Testing
DisplayPort Sources

DSO90000A Infinium Oscilloscope

W2641A DisplayPort Fixture

U7232A DisplayPort Compliance Test Software
Source Testing Solution Configuration

Infiniium Oscilloscope: DSA90804A (recommended)
  – Extended Memory: Option 001/002 optional
  – U7232A DisplayPort Compliance Software 6K$
  – 1169A Probe Amplifiers (4) OPTIONAL
  – N5380A Probe Heads (4) OPTIONAL

DisplayPort Fixture
  – W2641A 2.8K$
Introducing the U7232A DisplayPort Source Compliance Test Software for the Infiniium Family of Oscilloscopes

1. Multi-Lane/Multi-Bit Rate/ Multi-Level and Multi-PreEmphasis support
2. Device Definition Driven User Interface and Testing
3. Tests
   • Eye Diagram Test
   • Non-Pre-Emphasis Level Verification
   • Pre-Emphasis Accuracy
   • Intra pair skew
   • Inter pair skew
   • Differential Transition time test
   • Single ended rise and fall time mismatch
   • Non-ISI Jitter
   • ISI Jitter
   • AC Common Mode noise
   • Unit Interval
   • Main Link Frequency
   • Spread Spectrum Modulation Frequency
   • Spread Spectrum Modulation Deviation accuracy
   • Cable end Eye
   • Cable end jitter
   • Cable end equalization.
What Your Setup Might Look Like…

With Probe Amp and N5380A probe head

Direct A-B connection: no probe Amp or probe head
The W2641A

- Long ‘nose’ to allow simultaneous operation of DisplayPort interfaces
- Aux Channel/HPD available
- Calibration constructs for de-embedding
- 8GHz performance
- Price ~2.8K$
- Rx and Tx Test models
- Does NOT support Cable Test
- Cables phased matched to 2ps
- Right Angle SMP cables coming soon
DisplayPort Sink Testing

N4903A JBERT or 81250 ParBERT

N5990A opt. 155

BIT-DP-RTF-0001 (for calibration)

W2641A DisplayPort Fixture

Sink Device

Manual

N4915-006 ISI Generator

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Validation and Compliance Testing
DisplayPort Cables

86100C
Digital Communications Analyzer

N5301A
Vector Network Analyzer

DisplayPort Receptacle Fixtures and Calibration Boards Kit, BitifEye BIT-DP-CBL-0001
Let's Drive the U7232A....

The UI for the U7232A DisplayPort Compliance Application is Different... There is a Setup thread of screens to define the users device and test connection.
Setup Screen Thread

The very first thing is to inform the application what the DUT can do. Then select the test type...

Start Project: Project Information, Template

Test Process Setup

- **Test Mode**
  - Compliance Conditions Only
  - User Defined Conditions
  - Targeted Characterization Testing

- **Device Type**
  - Source
  - Differential Tests

Test Process: Identify Task
Setup Screen Thread

The next is to select the fixture type and the connection mode…

Test Connection: Fixture, Connections and Channels

DUT Definition: Device Capability Defined

Must Specify condition for Jitter Measurement
Setup Screen Thread

Blue square=OK

Drop Down selection Allows user to assign scope channels to lanes

Scope Channel Assignments
This screen is highly dependent on the parameters you have chosen before hand: For instance if you selected one lane to test you will NOT see ‘Lane 0’ and ‘Lane 1’ tests. Inter-skew test will not show up if you test with one channel at a time or if the DUT has only One channel! This eliminates common mistakes.
Configure

This screen is now dedicated for the CONFIGURABLE Parameters in Measurement Algorithms. You will NOT find scope channels or Lanes to test here ANYMORE.
Connection

Same High Detail for connection we have always provided

- Connect Lane0+ & Lane0- to SMA Probe Head (A).
- Attach SMA Probe Head (A) to InfiniiMax Probe Amplifier (A) and connect to Channel 1 of Infinium Oscilloscope.

- Connect Lane1+ & Lane1- to SMA Probe Head (B).
- Attach SMA Probe Head (B) to InfiniiMax Probe Amplifier (B) and connect to Channel 2 of Infinium Oscilloscope.

- Connect Lane2+ & Lane2- to SMA Probe Head (C).
- Attach SMA Probe Head (C) to InfiniiMax Probe Amplifier (C) and connect to Channel 3 of Infinium Oscilloscope.
More Sophisticated DisplayPort Testing
Product Development, Your Customers, and You

- Debug/Characterize
- System Tools Measurement
- System Debug
- Integration
- Debug
- Reference Design
- Certification
- Test
- Support
- Sales
- Product Proto, Beta...
- Design Guidelines
- Verification Tools
- Modeling
- Silicon Proto, Beta, 1st
- Test House, Test Process, Equipment
- Testing
- SW FW App sp
- Sys Tools
- Support Tools
- Time
- $$
- Timing Unc
- Design Guidelines

You

Your Customers
Testing the Source

These are the conditions that need to be tested for compliance. Optional configurations are demoted w/red x’s. Red test labels are informative tests and are NOT required.

Example: Test 3.2: All data rates, lanes and levels that apply to your DUT must be tested. Pre-emphasis is OFF for this test.

Potentially 64 jitter tests! Automation will be VERY welcome Here!
Compliance Test Specification: Sink Testing

Stressed Eye oriented
Fixed Level

Jitter components:
--Inter Symbol-Interference
--Sinusoidal Jitter swept.

Automation REQUIRED because generally Display vendors do not allow access to Rx chip error counter!
Testing

Source: DisplayPort test states include definition of:

- Pattern (D10.2 or PRBS7)
- Level (400, 600, 800, 1200 mVolts peak to peak)
- Pre-Emphasis (0, 3.5, 6, 9.5 dB)
- Bit Rate (1.62, 2.7 Gb/s)
- Lanes (0, 1, 2, 3)
- Spread Spectrum Clocking (Enabled, Disabled, Both)

Sink: DisplayPort enables error counting

- Error register validation and control
- Link Training
- PRBS7 stressed pattern, 2 bit rates, 4 sinusoidal frequencies
- 4 Lanes
AUX Channel Control (AUX Channel)

- Designated Control Link lane called ‘the AUX Channel’ specified. Operates at 1Mbs and is used in Link Training and Link Management and is Bidirectional Half Duplex.
- The Transmitter is the master.
- Receiver gains attention by pulling down on the Hot Plug Detect Line.
- Manchester II coding.
Achieving Standard Device Control and Automation

Driver

Logic Decode

Tx

AUX Channel Controller

Bit Recovery Lock

Err

DPCD

EDID
AUX Channel Controller - Key to DP Test Vision

- Aux Ch Sink Emulation
  - Fully programmable DPCD and EDID emulator
  - Accessed by DP Source over the Aux Channel
  - HPD generation and detection
  - LAN connection to instrument or PC provides full remote control of DPCD/EDID/HPD contents and function – key to automated test and debug

- AuxCh Source Emulation
  - Accesses DPCD and EDID in Sink Device via AuxCh port
  - HPD detect and generate
  - Enables communication with DP sink test registers to automate compliance and characterization
AUX Channel Controller

**Systems**

**DPTC Only**
- Standard GUI
- R/W EDID
- R/W DPCD
- API Command Logging

**Sink and Source**
- Factory Automation: N5990A Exclusive API for Source and Sink Testing

**Source Only**
- Source Testing: U7232A or N5990A Compliance Software
Automating Physical Layer Source Testing

U7232A V2.0

USB/LAN

DisplayPort Cable

BitifEye Software
N5990A opt. 255

DP DUT
Automating Physical Layer Sink Testing

Stressed Signal Generator

RTF needed for calibration and testing tethered cable devices

DisplayPort Cable

BitifEye Software N5990A opt. 155

LAN

DP DUT
Stressed Signal Generator

1) Based on ParBERT 7G TMDS Sig. Gen. E4887A-007

Upgrade to HDMI TMDS Signal Generator by adding 2 additional generator modules and 1 ESG
Stressed Signal Generator

2) J-BERT N4903A
Automated DisplayPort Compliance and Characterization

With Software Test Platform N5990A

Custom Solution

Test Sequencer

Legacy Code

Source-Test Software

Sink-Test Software

Instrument Software

Standard Instruments

Services (Partner Company BitifEye)

N5990A Test Automation Software Platform
(Opt. 010, Base Product)

N5990A Opt. 500 (MS .NET dlls)

Interface to N5399A
(N5990A Opt. 255)

NEW!

C++

C#

LabView, VEE

NEW!

…

DP-Tx

DP-Rx (Opt. 155)

DP-HDCP (Opt. 355)

DP-Cable (Opt. 455)

DP-else? (Opt. xyz)

Real-time Oscilloscope

ParBERT

J-BERT

Protocol Gen./Analyzer

TDR, Network A.

else?

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DUT Configuration

Configure Product

Product
- Product Number: DP-3000
- Serial Number: 123456789
- Product Type: Sink
- Port Name: 1
- Description: DP Receiver using Firmware Rev. 0.45
- Number of Lane(s): 1

Test
- User Name: Test Operator
- Comment:
- Initial Start Date: 11/26/2007 12:36:26 PM
- Compliance Mode
- Last Test Date: 11/26/2007 12:36:26 PM
- Expert Mode
- Sink PHY Test
  - Use Reverse PFBS7
  - Use dummy AUX Channel Controller
Connection Diagram Example
Calibration L0 ParBERT

Real Time Oscilloscope

Channel 1

Channel 4

Differential Probe

Shortcut

RF Out

Clk In

Delay Ctrl. Input

Clk Out

50Ω Termination

150ps TTCs

BIT-DP-RTF-0001 Receptacle Test Fixture

Aux Channel Controller

W2641A DisplayPort Fixture

L0+

L1-

L1+

L2+

L2-

L3+

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Connection Diagram Example
Calibration L0 J-BERT

![Diagram showing connections and components including Attenuator, Power Divider, Differential Probe, and Blocking Capacitor.](image-url)
Calibration Procedure Example

Common N5990A GUI
Connection Diagram Example
Jitter Tolerance Test Lane 1

DUT

Aux Channel Controller

W2641A DisplayPort Fixture

ISI Board

150ps TTCs

Blocking Capacitor / Bias-Tee Kit

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Expert Mode Characterization

Automated Sink Test Calibration

Jitter Tolerance at High and Reduced Bit Rate (HBR, RBR) @ 10 and 20 MHz

separate 2 MHz HBR and RBR and 100 MHz SJ HBR Tests

Jitter Tolerance Characterization

Sensitivity and Skew test
Expert Mode
Variable Parameter Test

User-selectable swing, SJ and RJ
Jitter Tolerance Characterization (Expert Mode)

This test goes over the specified frequency range and increases the SJ until the target error number is reached.

![Jitter Tolerance Graph]

- **Jitter Tolerance**

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Agilent DisplayPort Test Solutions w/ACC

Source Test Solution
Computer Motherboards, ICs, Graphic Cards
- DSO90000A Infinium Real Time Oscilloscopes
- U7232A DisplayPort Compliance Test SW
- W2641 TPA fixture

Media Testing
Cables, PC Boards, Connectors
- 86100C DCA-J DisplayPort
- E5071C VNA
- W2641A TPA fixture
- Bit-DP-CBL-0001

Sink Test Solution
PC Monitors
- N4903A JBERT, ParBert
- N4915A -006 DP ISI Generation
- N5990A Rx Compliance Test SW
- W2641A TPA fixture
- Bit-DP-RTF-0001

Link Layer & General Solutions

Agilent DisplayPort Test Solutions w/ACC
AUX Channel Controller GUI (Setup)

To test complex devices, 2 or more DPTCs could be used.

Supports varying Hot Plug Event lengths.
AUX Channel Controller GUI (EDID Read and Write)

Can act like a sink (with a library of displays)
Or can act like a source and read the values
The DPCP is quite lengthy although little of it is used.

Can read and write to individual addresses
AUX Channel Controller GUI (Extension: Scripting) FUTURE Capability

Can create desired flow with library of functions. Conditionals on # of times, values, etc.

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th>In/Out1</th>
<th>In/Out2</th>
<th>In/Out3</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Read EDID</td>
<td>Get Version</td>
<td>All Working Commands</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>*Set State</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>*Set Mode</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Define Variable</td>
<td>Get Version</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>*Read EDID</td>
<td>Get State</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Error: repeat</td>
<td>Get Version</td>
<td>Get Mode</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Error: goto</td>
<td>Repeat last n</td>
<td>Repeat last n</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Add to Variable</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>Repeat last n</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>LED: Green</td>
<td></td>
<td></td>
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</table>

GUI Version 1.20 Firmware Version?
AUX Channel Controller GUI (Extension: Logging)

Logs all API traffic

```
dpt_set_mode(DPT_MODE_SINK_EMULATION_1) = 0x80000001
```
Testing a Repeater
# DisplayPort Solution Ordering Configuration

<table>
<thead>
<tr>
<th>Model #/Opt</th>
<th>Description</th>
<th>Ref. Price</th>
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</thead>
<tbody>
<tr>
<td>Source Test</td>
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<tr>
<td>DSA90804A</td>
<td>Infiniium Oscilloscope</td>
<td>$85K</td>
</tr>
<tr>
<td>U7232A</td>
<td>DisplayPort compliance Test software</td>
<td>$6K</td>
</tr>
<tr>
<td>W2641A</td>
<td>DisplayPort Test Point Adaptor</td>
<td>$2.5K</td>
</tr>
<tr>
<td>1169A</td>
<td>Infiniimax Probe Amplifiers (optional)</td>
<td>$9K$</td>
</tr>
<tr>
<td>N5380A</td>
<td>Differential SMA Probe Heads</td>
<td>$2.4K</td>
</tr>
<tr>
<td>tbd</td>
<td>DisplayPort Test Controller</td>
<td>tbd</td>
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<td>Sink Test (J-BERT)¹</td>
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<tr>
<td>N4903A</td>
<td>JBERT-C07</td>
<td>$131K</td>
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<tr>
<td>Opt J20</td>
<td>ISI and PJ Injection</td>
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<td>Opt J10</td>
<td>Jitter Injection</td>
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<td>BIT-DP-RTF-0001</td>
<td>DisplayPort Test Point Adaptor Receptacle</td>
<td>$5K</td>
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<tr>
<td>N5990A</td>
<td>Factory Automation Software, option 010,155 (options 001 and 255 recommended)</td>
<td>$20K (+$15k)</td>
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<td>N4915-006</td>
<td>DisplayPort ISI Generator</td>
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<td>11636B</td>
<td>Power Divider</td>
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<td>11667B</td>
<td>Power Splitter (qty. 2)</td>
<td>$2.8K</td>
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<tr>
<td>15435A</td>
<td>Transition Time Converters 150 ps (qty. 4)</td>
<td>$1.6K</td>
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<tr>
<td>N9398C</td>
<td>Blocking Capacitors (qty. 6)</td>
<td>$1.5K</td>
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<td>E4809-61603</td>
<td>SMP-to-SMA cables, right-angle (qty. 6)</td>
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<td>tbd</td>
<td>DisplayPort Test Controller</td>
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¹) Contact Agilent for ParBERT configuration
Support Resources

Top Sales Tools/ Resources Agilent DisplayPort Solutions

- Infiniium 90000 Series Oscilloscopes 5989-7819EN
- U7232A DisplayPort Compliance Data Sheet 5989-7198EN
- N4903A JBERT Data Sheet 5989-2899EN
- DisplayPort Sink Test Application Note 5989-9147EN
- W2641A DisplayPort Test Point Adaptor Data Sheet 5989-7247EN
- N5990A Test Automation Software Platform Data Sheet 5989-5483EN

Website to Access Sales Support Resources

- www.agilent.com/find/DisplayPort