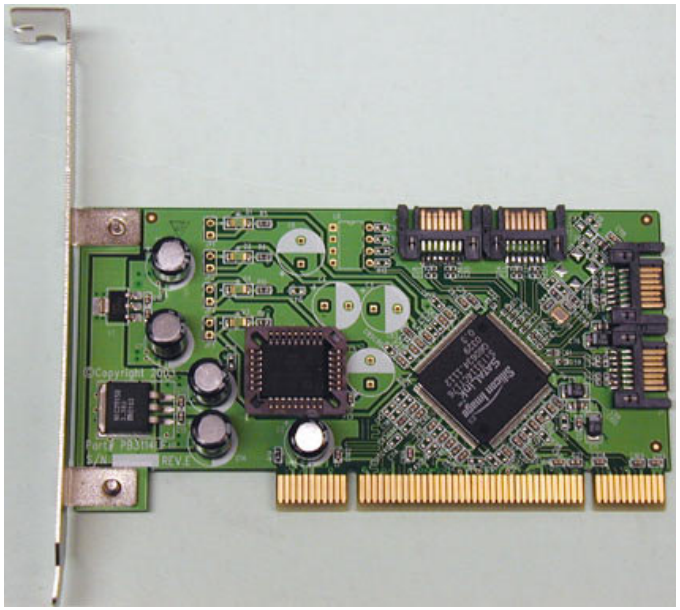
Serial ATA Validation and Compliance Solutions:

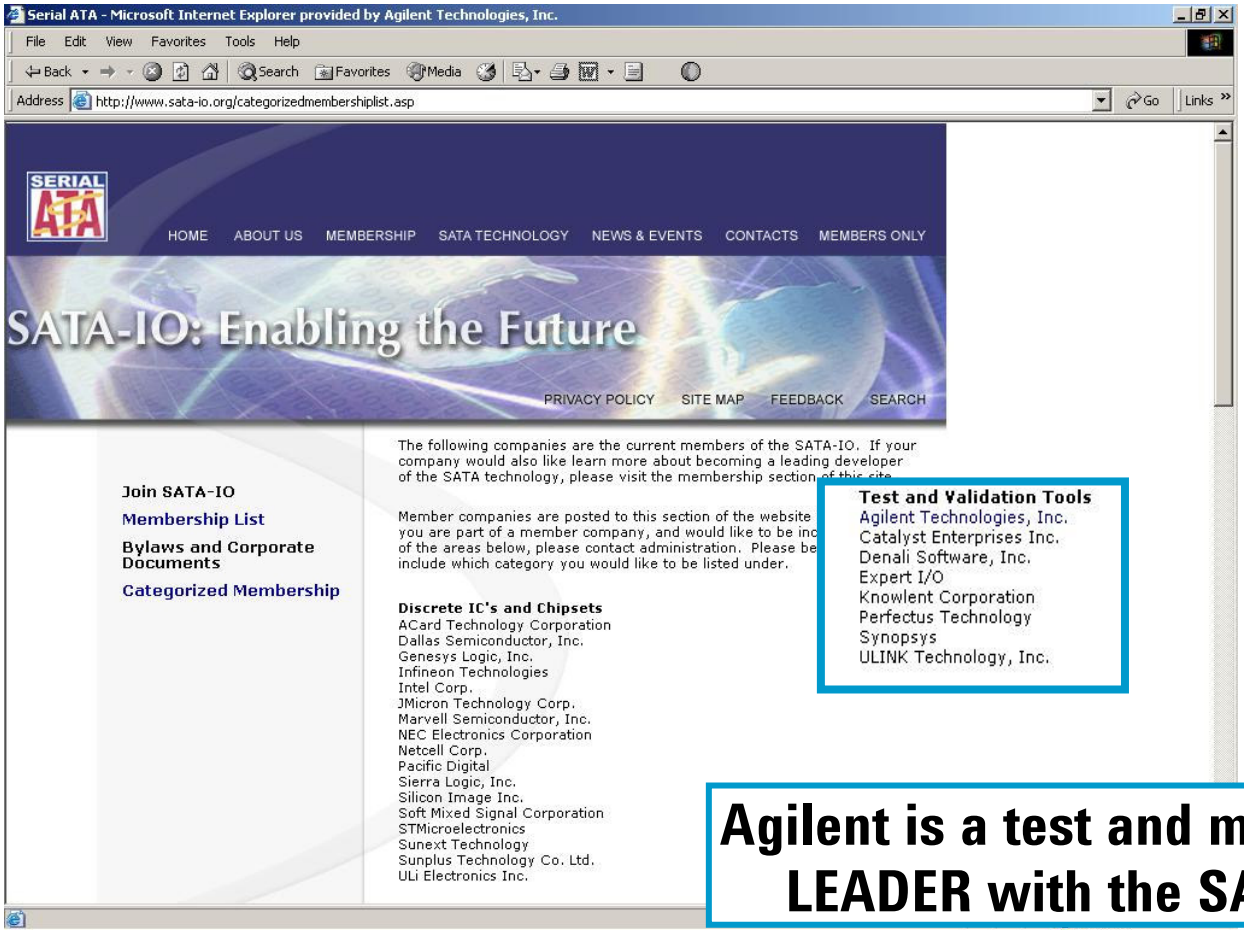
Agilent Technologies

Serial ATA

Serial ATA is a replacement for the existing ATA drive attachment interface with forward-looking provisions for higher data throughput and a broader connectivity offering.

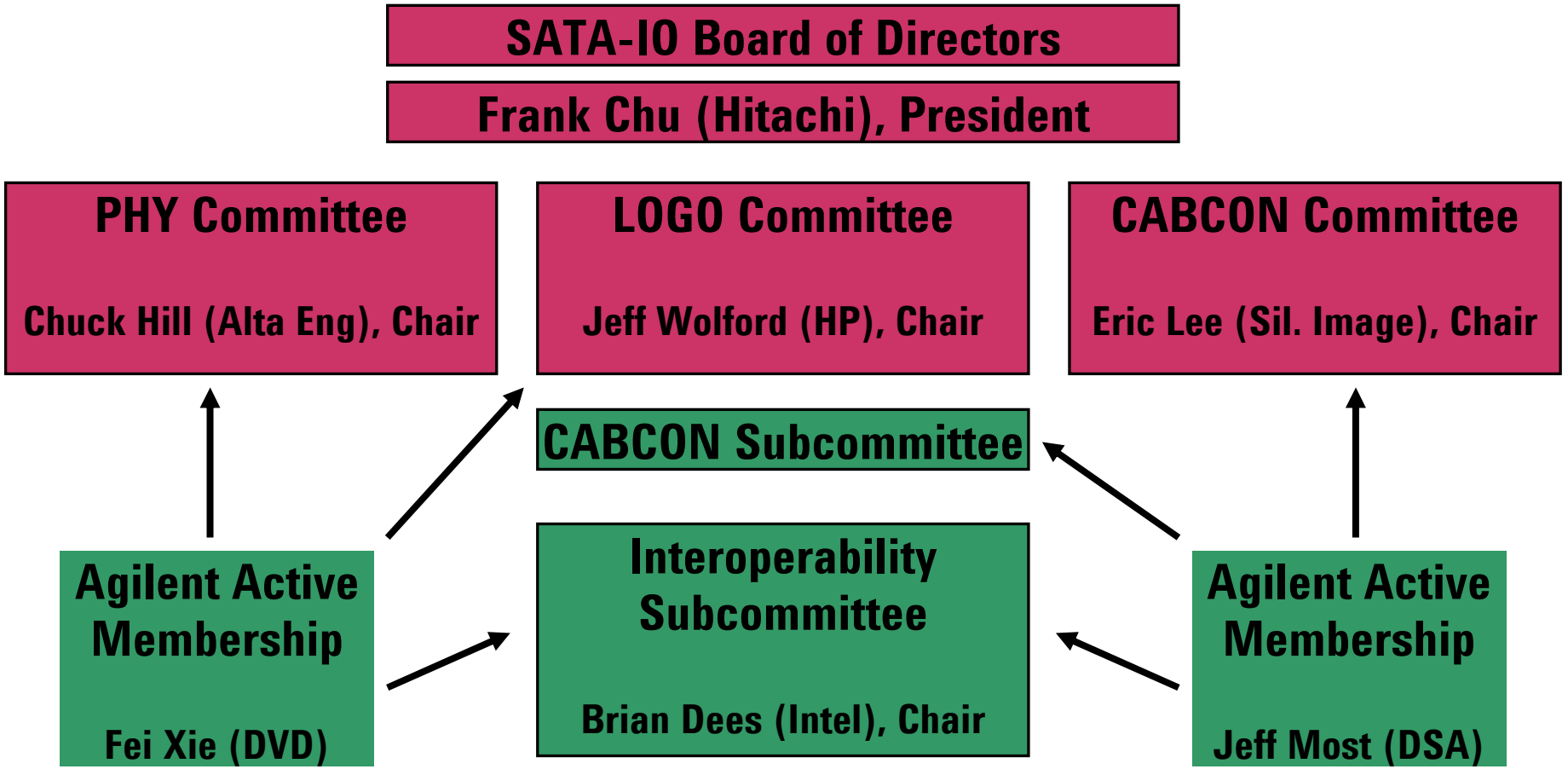


SATA-IO Membership and Participation



Agilent is a test and measurement LEADER with the SATA-IO!!!

Serial ATA International Organization (SATA-IO)



SATA-IO LOGO Interoperability Workshop Policy

Unified Test Document

- The Unified Test Document is the guiding policy document for official SATA-IO device testing at the Interoperability Workshops, and is currently at revision 1.2 (Feb 2007)
- As of February 2007, only Agilent and Tektronix are actively participating in the weekly LOGO discussions that define the IW policy and test requirements
- Only active participants and contributors will be approved and accepted on the Approved Vendors List.
- Both Agilent and Tek have approved MOIs.
- Lecroy seems to have no intentions of creating MOIs.

SATA-IO LOGO Interoperability Workshop Major Updates

- An important change has occurred in the past months that has moved the Interoperability Workshop testing method for Gen 1 jitter away from the legacy 5UI/250UI test method. **Gen 1 and Gen 2 jitter are now both measured using a TIE based method** (EZJIT Plus) that can accurately measure DJ and TJ at a BER of 10^{-12}. This change is documented in the Unified Test Document ver1.2

- The SATA-IO now requires that equipment to meet return loss requirements. **Agilent scopes are the only real time scopes that meet these.** Tek show in their PHY-TSG-OOB-MOI ver1.1 the use of a 6dB attenuator at the front end of the scope for all measurements in order to have a setup that meets requirements. Agilent includes in their PHY-TSG-OOB-MOI ver1.1 lab load data that shows we meet the requirement.

- **Receiver testing** has will be required for the first time at the IW #3 in May 07.

Agenda

- **Transmitter (TX) Validation**
  - Specification Compliance Testing
  - Jitter Margin Testing
  - Eye Diagram Mask Template Testing
  - Bit Failure Analysis
  - Spread Spectrum Clock (SSC) Accuracy Testing
- **Receiver (RX) Validation**
  - Stressed Eye Diagram Testing
- **Full Compliance Test Suite**
  - ValiFrame Software: Simplifying Test with Automation

Agenda

- **Transmitter (TX) Validation**
  - Specification Compliance Testing
  - Jitter Margin Testing
  - Eye Diagram Mask Template Testing
  - Bit Failure Analysis
  - Spread Spectrum Clock (SSC) Accuracy Testing
- **Receiver (RX) Validation**
  - Stressed Eye Diagram Testing
- **Full Compliance Test Suite**
  - ValiFrame Software: Simplifying Test with Automation

Ever Increasing Speed

Signal Integrity Issues

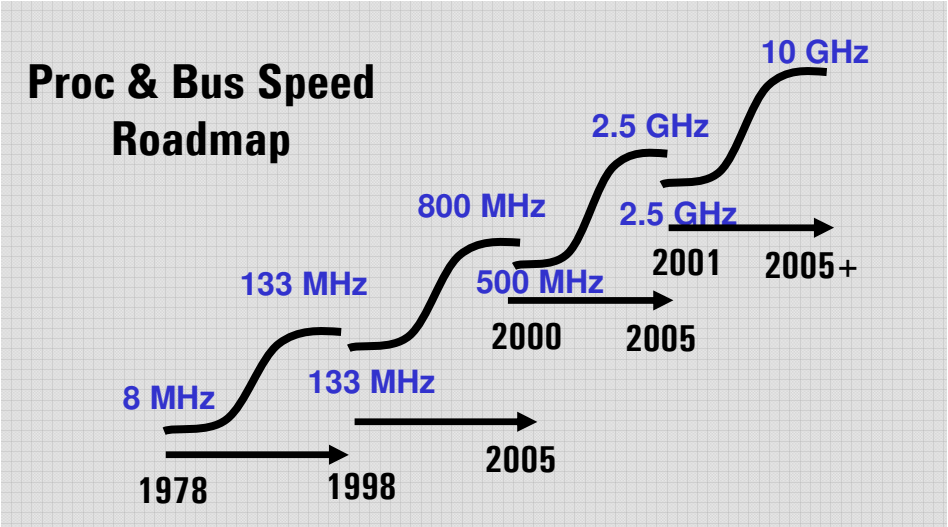
Clock Speeds >2 GHz

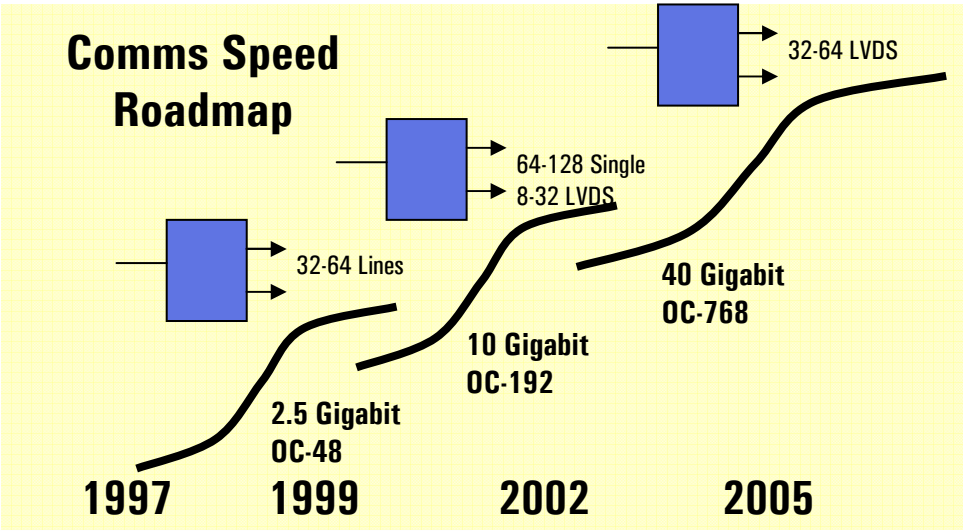
Edge Rates <100 ps

Crosstalk, Impedance, EMI, and Jitter measurements

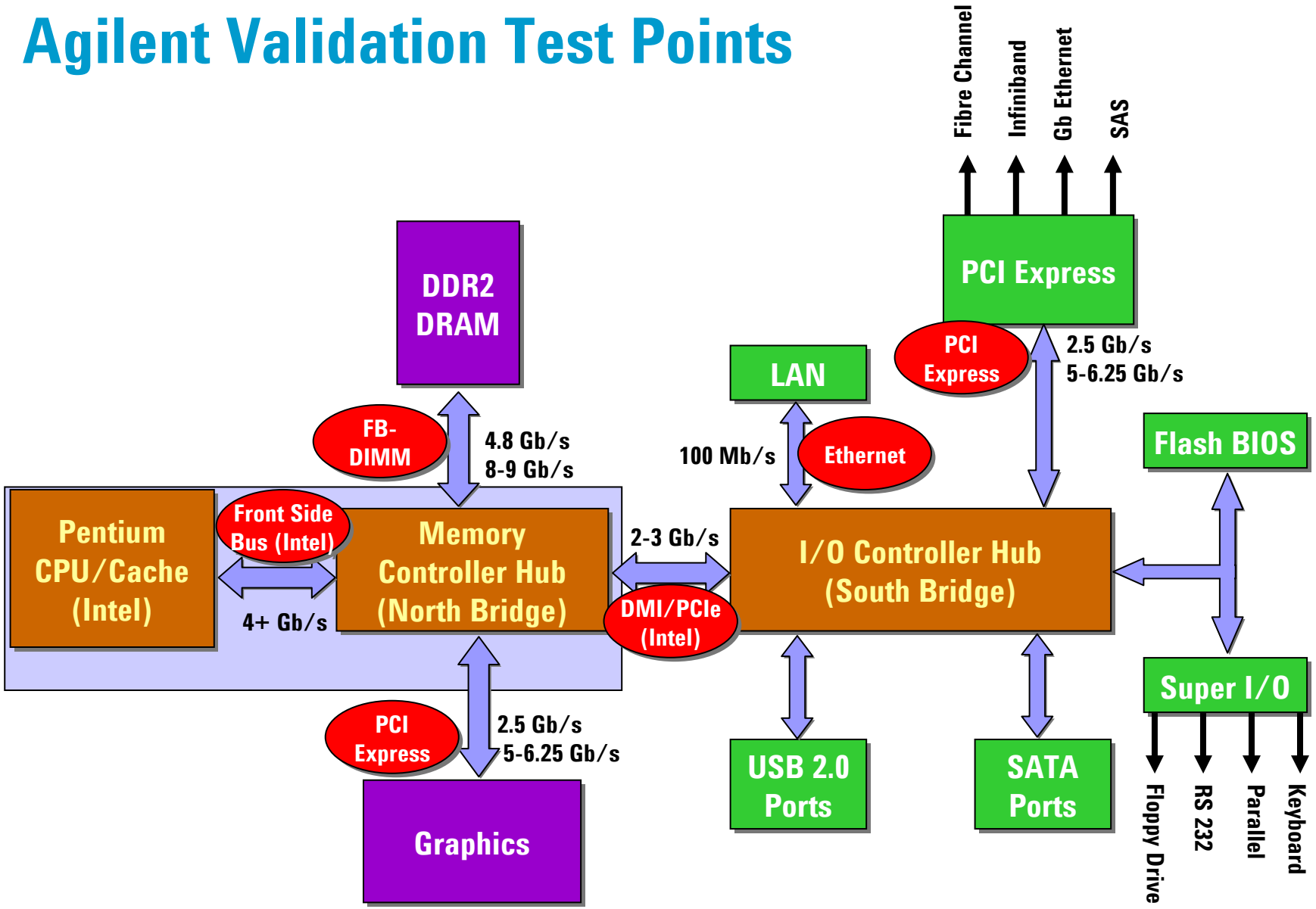
Channel modeling is required

I'm becoming a microwave designer





Agilent Validation Test Points

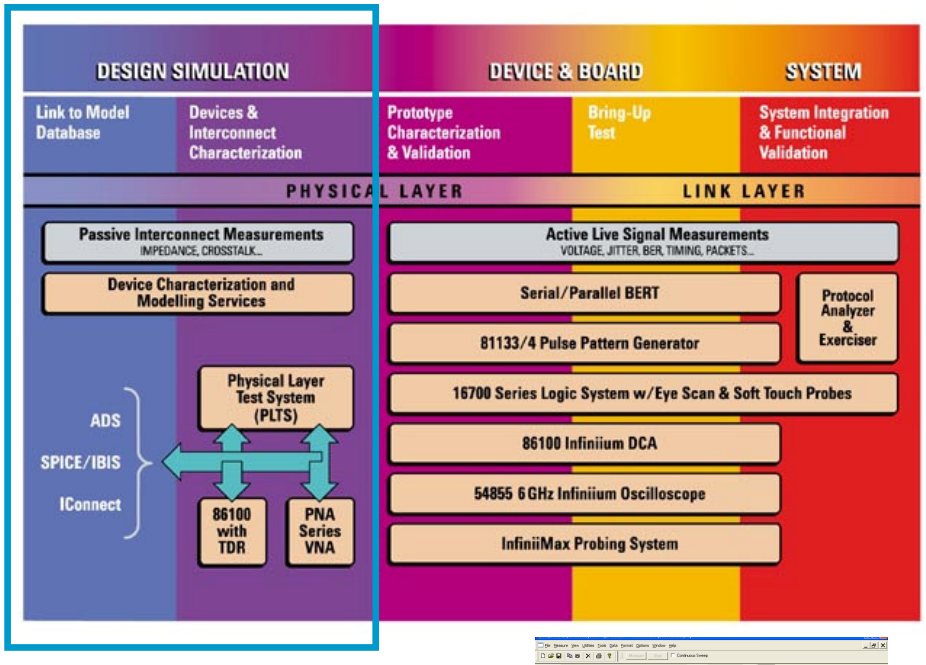


Bandwidth Requirements for New Standards

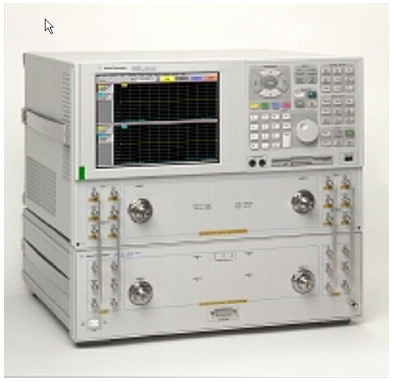
Popular Apps	Signal Rate	Fundamental Freq	Rise Time		Optimum Bandwidth	
			Base (at GBA)	CEM/Probing Point	Brickwall	Gaussian
USB2.0	480Mbps	240MHz	500ps (10-90%)		1.5GHz	2.0GHz
DDR2	Up to 800MT/s	400MHz	288ps (10-90%)		2.4GHz	3.3GHz
DDR3	Up to 1.6GT/s	800MHz	120ps (10-90%)		5.8GHz	7.9GHz
Serial ATA I	1.5Gbps	750MHz	100ps		5.6GHz	7.9GHz
Serial ATA II	3Gbps	1.5GHz	67ps		8.4GHz	11.3GHz
SAS150	1.5Gbps	750MHz	67ps		8.4GHz	11.3GHz
SAS300	3Gbps	1.5GHz	67ps		8.4GHz	11.3GHz
SAS600	6Gbps	3GHz	47.7ps		11.7GHz	15.9GHz
PCI Express Gen I	2.5Gbps	1.25GHz	50ps	100ps	5.6GHz	7.9GHz
PCI Express Gen II	5Gbps	2.5GHz	45ps	Not Available Yet	12.5GHz	17GHz
ExpressCard	2.5Gbps	1.25GHz	50ps	100ps	5.6GHz	7.9GHz
Fibre Channel 4G	4.25Gbps	2.125GHz	75ps		7.5GHz	10.1GHz
Fibre Channel 8G	8.5Gbps	4.25GHz	60ps		9.3GHz	12.7GHz
XAUI	3.125Gbps	1.5625MHz	60ps		9.3GHz	12.7GHz
HDMI 1.3	3.4Gbps	1.7GHz	75ps		7.5GHz	10.1GHz
DVI	1.65Gbps	825MHz	75ps		7.5GHz	10.1GHz
DisplayPort	2.7Gbps	1.35GHz	75ps		7.5GHz	10.1GHz
FBD I	4.8Gbps	2.4GHz	35ps	45ps	12.5GHz	17GHz
FBD II	9.6Gbps	4.8GHz	25ps??	45ps	12.5GHz	17GHz
CSI Gen I	Contact Division. CSI is Intel confidential information					
CSI Gen II						

- New standards require higher BW meas. capability and analysis tools
- Probing, channel analysis and modeling will be critical for success

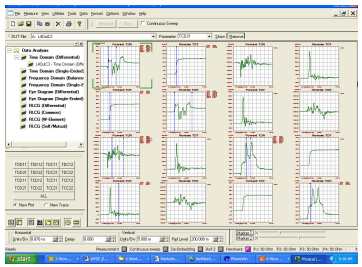
Interconnect Characterization Solutions



50 GHz VNA



PLTS



86100 DCA/TDR

Focus:

Optimize interconnects for signal transmission

Products:

86100 DCA/TDR

PNA Series VNA

N1930 PLTS

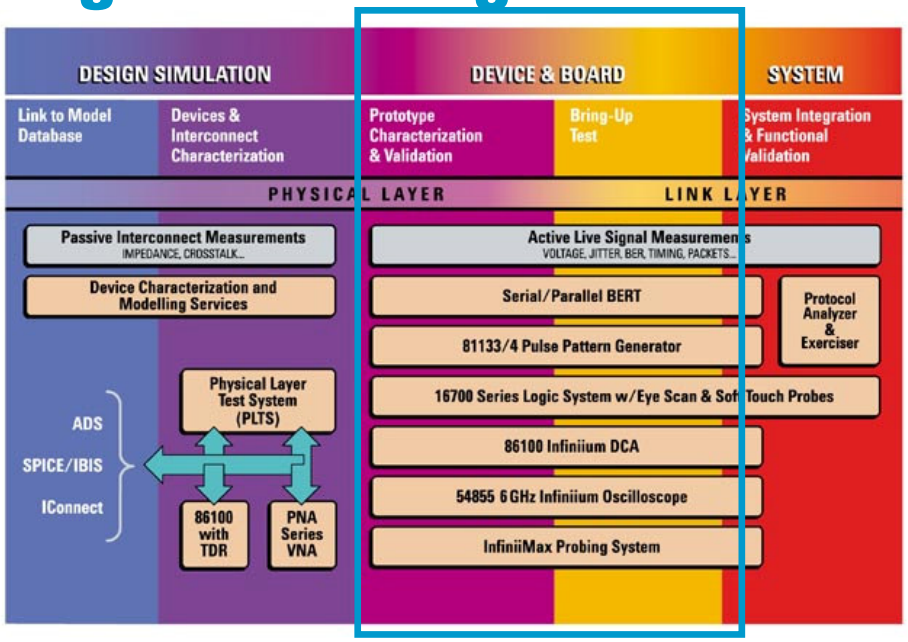
ADS

Benefits:

Determine proper impedances to minimize crosstalk and signal quality problems

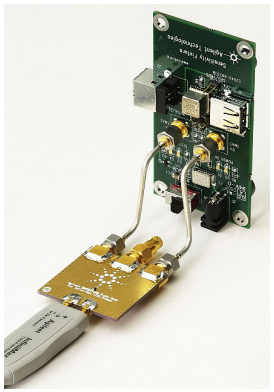
Link to simulations tools

Signal Probing Solutions



InfiniiMax Probes

N5380A SMA Adapter



N1022 Adapter for DCA

Focus:

Measuring the right signal via quality probing

Products:

1160 Series InfiniiMax II Probes

DSO 80000 Real-time Scope

86100 DCA

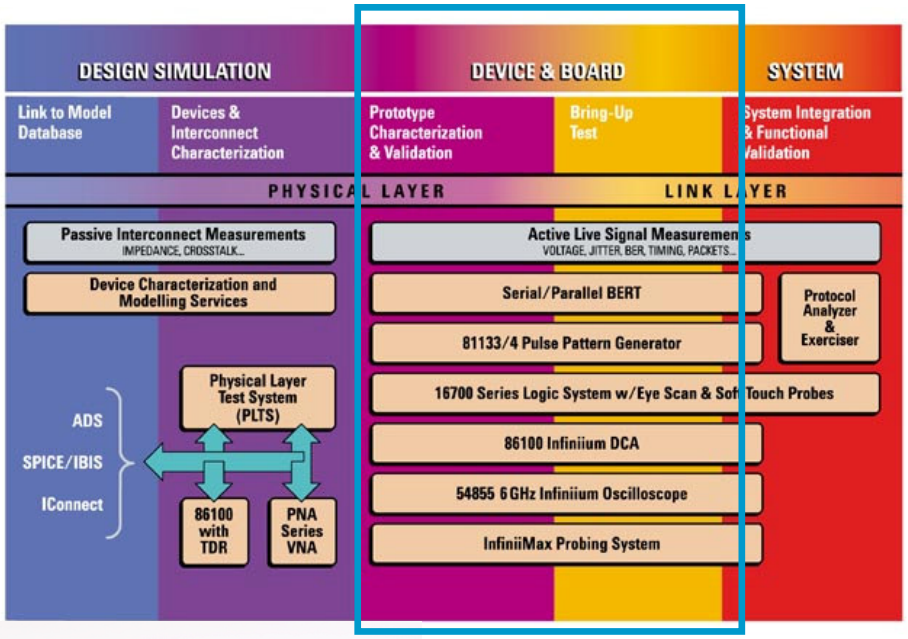
8113x Pulse Generators

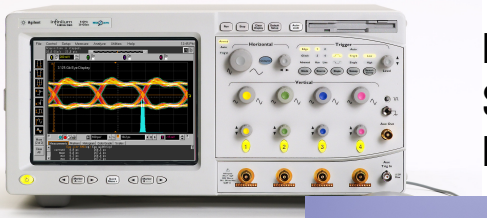
Benefits:

Low loading and flat response give you the best view of your signal without disrupting system operation

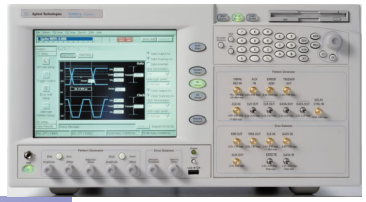
Differential probing for > CMRR

Jitter Measurement Solutions





DSO 80000
86100 DCA



N4901 Serial BERT

81134 PG

ParBERT

Focus:

Jitter Characterization

Products:

DSO 80000 Real-time Scope

86100 DCA-J

N4900 Serial BERTs

81250 ParBERT

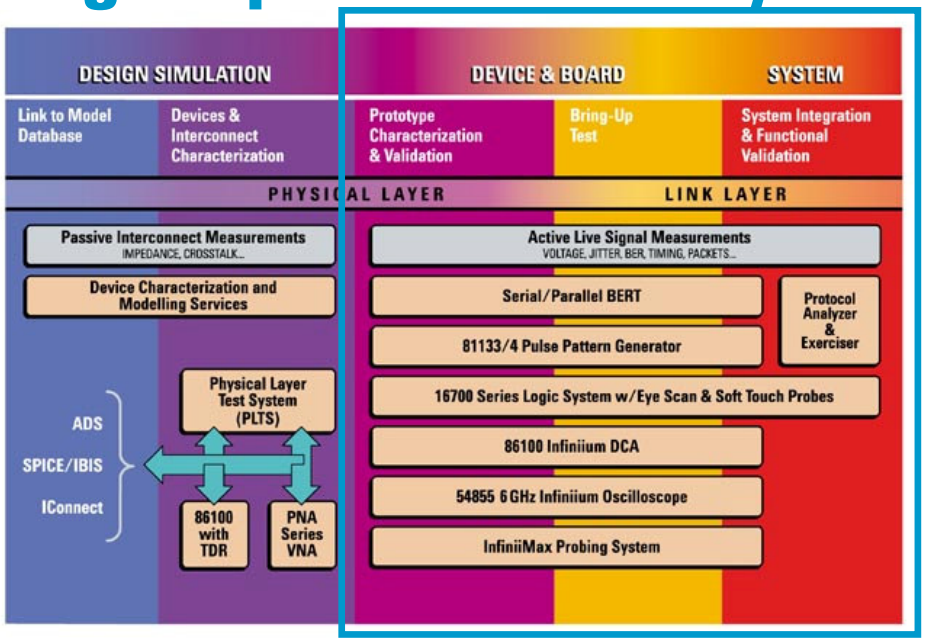
8113x/4x Pulse Generators

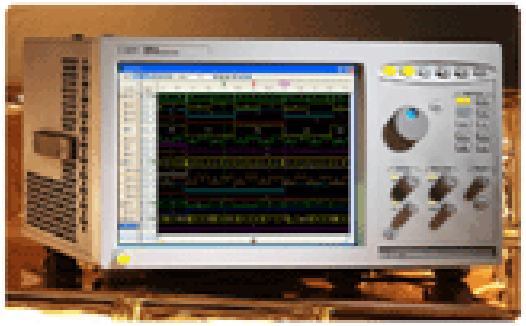
Benefits:

Jitter measurement coverage of SONET and MJSQ standards

Select the optimum measurement solution for your design

High-Speed Bus Analysis Solutions





16900 Logic Analyzer

E2960 Protocol Analyzer

Focus:

Bus analysis, stress and compliance test

Products:

16900 Series Logic Analyzer

E2960 Protocol Analyzer & Exerciser (PCI Express)

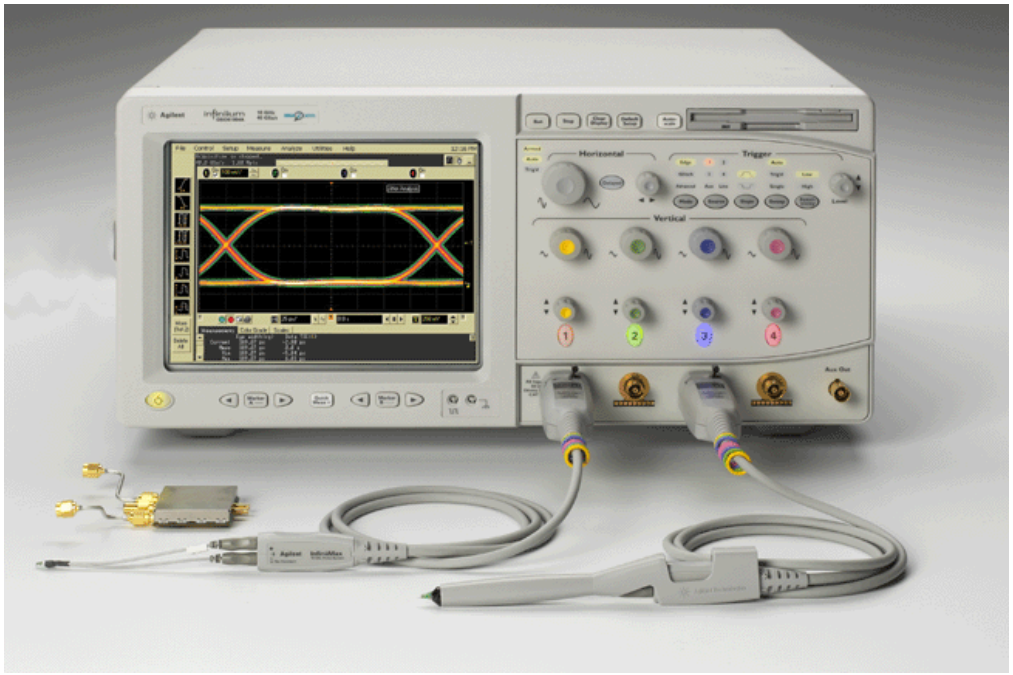
DSO 80000 Real-time Scope

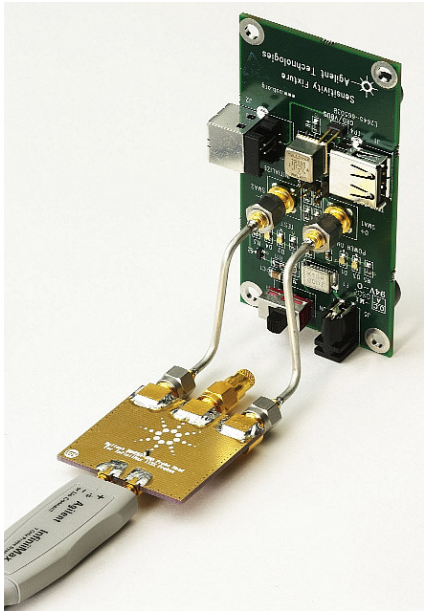
Benefits:

Characterize the latest high-speed buses, both early debug and final system test

PCIe Compliance Test Card

Infiniium DSO 80000B Series Oscilloscopes





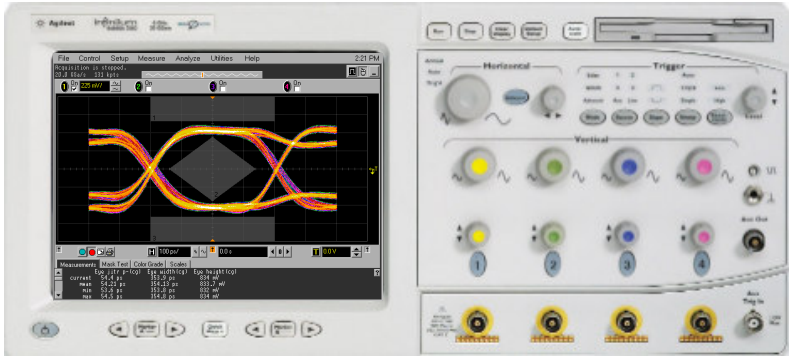
2,3,4,6,8, 10, 12 and 13 GHz Scope Models

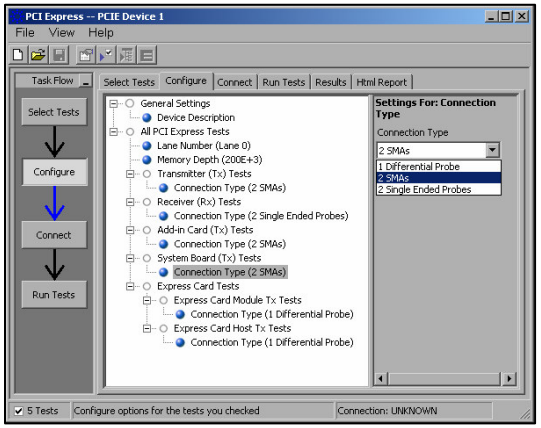
Upgradable Bandwidth / Lowest NoiseFloor

10 and 12 GHz InfiniiMax II Active Probe models

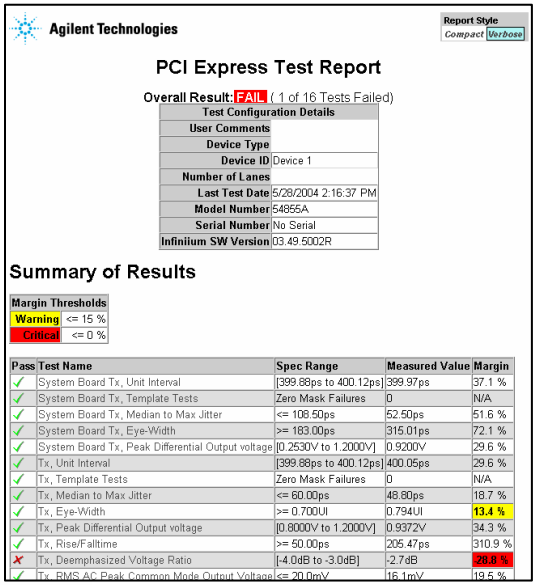
12 GHz SMA, ZIF, Solder-in and Browser probe heads

High-Performance Oscilloscope Tools





- N5393A PCI Express Electrical Compliance & Validation Software PCI Express 1.0a & 1.1
- E2688A High-Speed Serial Data Analysis
- N5400A EZJIT Plus Jitter Analysis Software
- N5411A SATA Electrical Compliance & Validation Software
- N5412A SAS Electrical Compliance & Validation Software
- N5392A Ethernet Electrical Compliance & Validation Software (10-, 100-, 1000Base-T)
- N5395A Ethernet Test Fixture
- N5396A Gigabit Ethernet Jitter Test Cable
- N5394A DVI Electrical Compliance & Validation Software
- N5313A DDR II Clock Characterization Tool



Agenda

- **Transmitter (TX) Validation**
  - **Specification Compliance Testing**
  - Jitter Margin Testing
  - Eye Diagram Mask Template Testing
  - Bit Failure Analysis
  - Spread Spectrum Clock (SSC) Accuracy Testing
- Receiver (RX) Validation
  - Stressed Eye Diagram Testing
- Full Compliance Test Suite
  - ValiFrame Software: Simplifying Test with Automation

N5411A Product Definition

The N5411A SATA II Electrical Compliance Test application:

- **Supports Gen 1(1.5Gbps) and Gen 2(3Gbps) data rates**
- **Supports the i, m and x Transmit (TX) interfaces**
- **Provides automated 81134A stimulus for OOB signal tests**

Our view of a complete solution includes:

- **Automated compliance test and verification software**
- **Lab-quality reference test fixtures to connect to the compliance interface**
- **Standards body representation and Inter-op plugfest support**

N5411A DUT Configuration Requirement

The N5411A SATA II Electrical Compliance Test application:

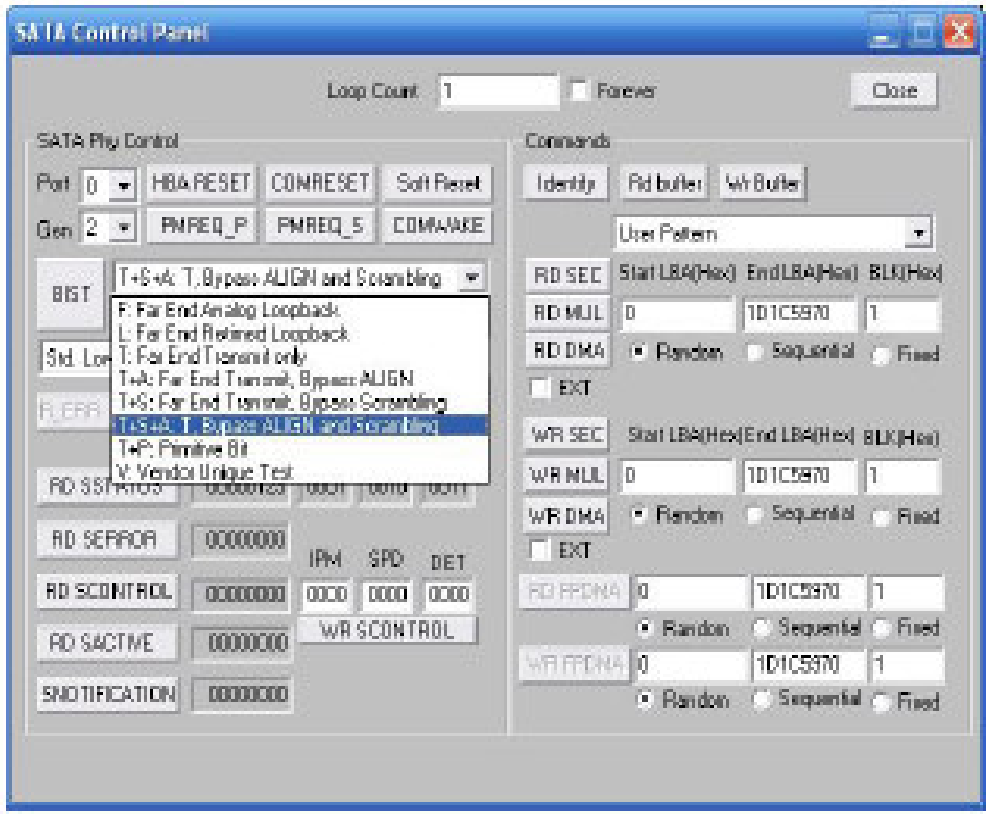
•REQUIRES that the PHY (DUT) be able to generate the COMP, HFTP, LFTP, MFTP and LBP compliance test patterns as per section 6.1.11 and section 6.2.4.3 of the Serial ATA II Electrical Specification 1.0 (http://www.sata-io.org).

OR

•That the PHY (DUT) be able to enter far-end retimed loopback mode as per section 6.2.3.1 of the Serial ATA II Electrical Specification 1.0 (http://www.sata-io.org).

DriveMaster as a BIST Enabling Tool: http://www.ulinktech.com

BIST Mode Test



Support Features:

- Port Select, Speed Down Shift
- HBA Reset, ComReset, SoftReset
- SATA Error counter
- User Define Loop Count

- **BIST Mode Test including:**
  - F: Far End Analog Loopback
  - L: Far End Retimed Loopback
  - T: Far End Transmit only
  - T+A: Far End Transmit, Bypass ALIGN
  - T+S: Far End Transmit, Bypass Scrambling
  - T+S+A: T, Bypass ALIGN and Scrambling
  - T+P: Primitive Bit
  - Vendor Unique Test

- Almost every silicon vendor supports either BIST-T,A,S or BIST-L test modes
- Those who do can use DriveMaster to enable standard test mode

N5411A Product Configuration Requirement

The N5411A SATA II Electrical Compliance Test application:

- **REQUIRES E2688A Serial Data Analysis Software (option 003)**
- **REQUIRES N5400A EZJIT Plus Software (option 004)**
- **REQUIRES H303000202 COMAX iSATA device TX/RX test fixture, distributed by CRUZ Systems (see page 30 for details)**

N5411A Product Definition

Test support:

Table 20 : General Specifications, page 131	Gen1i	Gen1m	Gen1x	Gen2i	Gen2m	Gen2x
Channel Speed	x	x	x	x	x	x
Tui, Unit Interval	x	x	x	x	x	x
Ftol, TX Frequency Long Term Stability						
Fssc, Spread-Spectrum Modulation Frequency	x	x	x	x	x	x
SSCtol, Spread-Spectrum Modulation Deviation	x	x	x	x	x	x
Vcm,dc, dc Coupled Common Mode Voltage	x	x				
Vcm,ac Coupled, ac Coupled Common Mode Voltage				x	x	

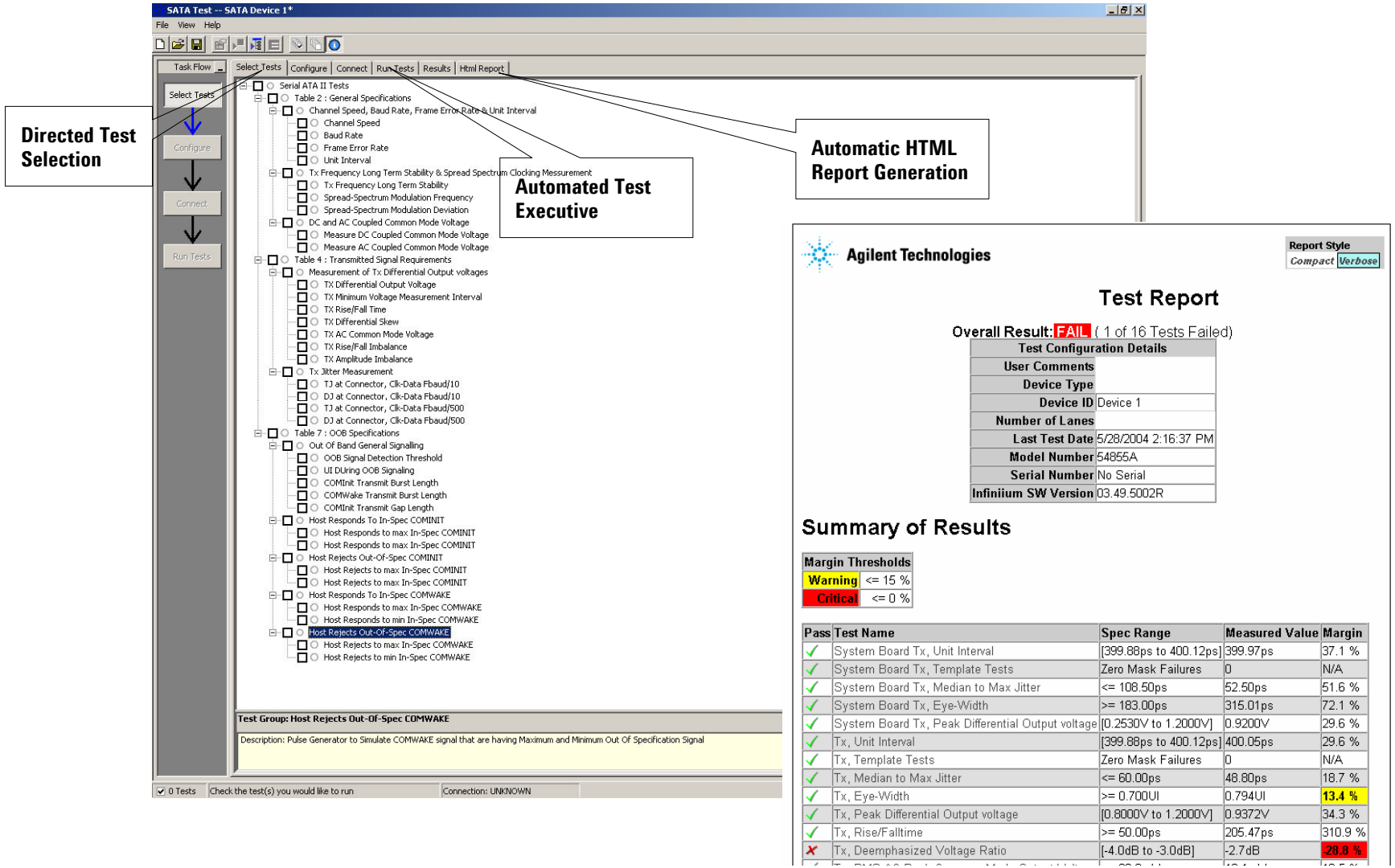
Table 25 OOB Specifications, page 140	Gen1i	Gen1m	Gen1x	Gen2i	Gen2m	Gen2x
UIOOB, UI During OOB Signaling	x	x	x	x	x	x
COMINIT/COMRESET and COMWAKE Transmit Burst Length	x	x	x	x	x	x
COMINIT/COMRESET Transmit Gap Length	x	x	x	x	x	x
COMWAKE Transmit Gap Length	x	x	x	x	x	x
COMWAKE Gap Detection Windows	x	x	x	x	x	x
COMINIT/COMRESET Gap Detection Windows	x	x	x	x	x	x

N5411A Product Definition

Test support:

Table 22 : Transmitted Signal Requirements, page 135	Gen1i	Gen1m	Gen1x	Gen2i	Gen2m	Gen2x
VdiffTX, TX Differential Output Voltage	x	x	x	x	x	x
T20-80TX, TX Rise/Fall Time	x	x	x	x	x	x
tskewTX, TX Differential Skew	x	x	x	x	x	x
Vcm,acTX, TX ac Commn Mode Voltage				x	x	
R/Fbal, TX Rise/Fall Imbalance				x	x	
TJ at Connector, Data-Data, 5UI						
DJ at Connector, Data-Data, 5UI	x	x				
TJ at Connector, Data-Data, 250UI	x	x				
DJ at Connector, Data-Data, 250UI	x	x				
TJ at Connector, Clk-Data, fBAUD/10						
DJ at Connector, Clk-Data, fBAUD/10						
TJ at Connector, Clk-Data, fBAUD/500				x	x	
DJ at Connector, Clk-Data, fBAUD/500				x	x	
TJ at Connector, Clk-Data, fBAUD/1667			x			x
DJ at Connector, Clk-Data, fBAUD/1667			x			x

Agilent N5411A SATA Electrical Compliance Tool

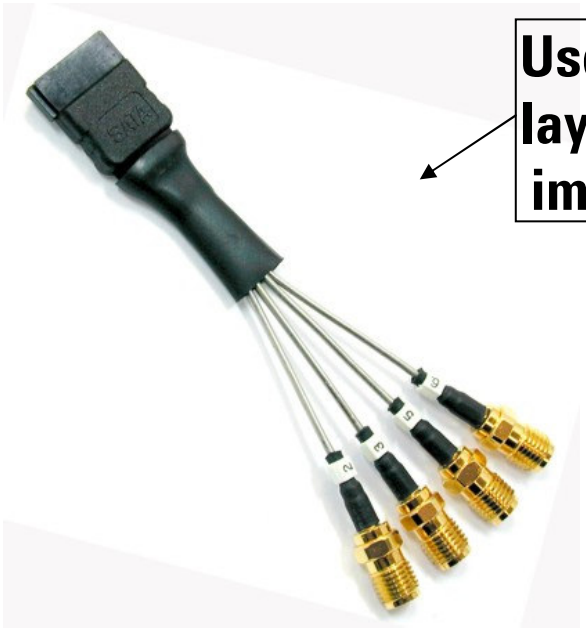


SATA I/II Test Fixtures

MUST Purchase H303000202 iSATA test fixture, distributed by CRUZ Systems to use N5411A Test Software

Far End Test Fixture (cable)

H303000202-G iSATA Test Fixture (Drive/Host)



Near End Test Fixture (Drive, HBA)

H303000102-G iSATA Text Fixture (Cable)

Available From Comax: www.comaxtech.com

Quick Comparison by Vendor

Test Parameter	Agilent	Tek
General Measurements		
Channel Speed	Y	Y
FBaud	Y	Y
Tui, Unit Interval	Y	Y
Ftol, Long Term Frequency Tolerance	Y	Y
Fssc, SSC frequency	Y	Y
SSCtol, SSC Modulation Deviation	Y	Y
Vcmdc, DC coupled Common Mode Voltage	Y	Y
Vcmac, AC coupled Common Mode Voltage	Y	Y
Transmitted Signal Requirements		
VdiffTx, Tx Differential Output Voltage	Y	Y
T2080Tx, Rise and Fall Time	Y	Y
Tskew, Tx differential skew	Y	Y
Vcmactx, Tx AC Common Mode Voltage	Y	Y
Amp bal, Tx Amplitude Imbalance	Y	Y
Tj Connector, Data-Data, Gen 1i/1m, 5UI	Y	Y
Dj Connector, Data-Data, Gen 1i/1m, 5UI	Y	Y
Tj Connector, Data-Data, Gen 1i/1m, 250 UI	Y	Y
Dj Connector, Data-Data, Gen 1i/1m, 250 UI	Y	Y
Tj Connector, Clock-Data, Gen 2i/2m, fbaud/10	Y	Y
Dj Connector, Clock-Data, Gen 2i/2m, fbaud/10	Y	Y
Tj Connector, Clock-Data, Gen 2i/2m, fbaud/500	Y	Y
Dj Connector, Clock-Data, Gen 2i/2m, fbaud/500	Y	Y
Tj After CIC, Clock-Data, Gen 1x/2x, fbaud/1667	Y	Y
Dj After CIC, Clock-Data, Gen 1x/2x, fbaud/1667	Y	Y
Out of Band Signal Testing		
COMINIT (Device)	Y	Y
COMRESET (Host)	Y	Y
COMWAKE (Host/Device)	Y	Y

No vendor wins on number of tests we can perform.

Agilent wins on:

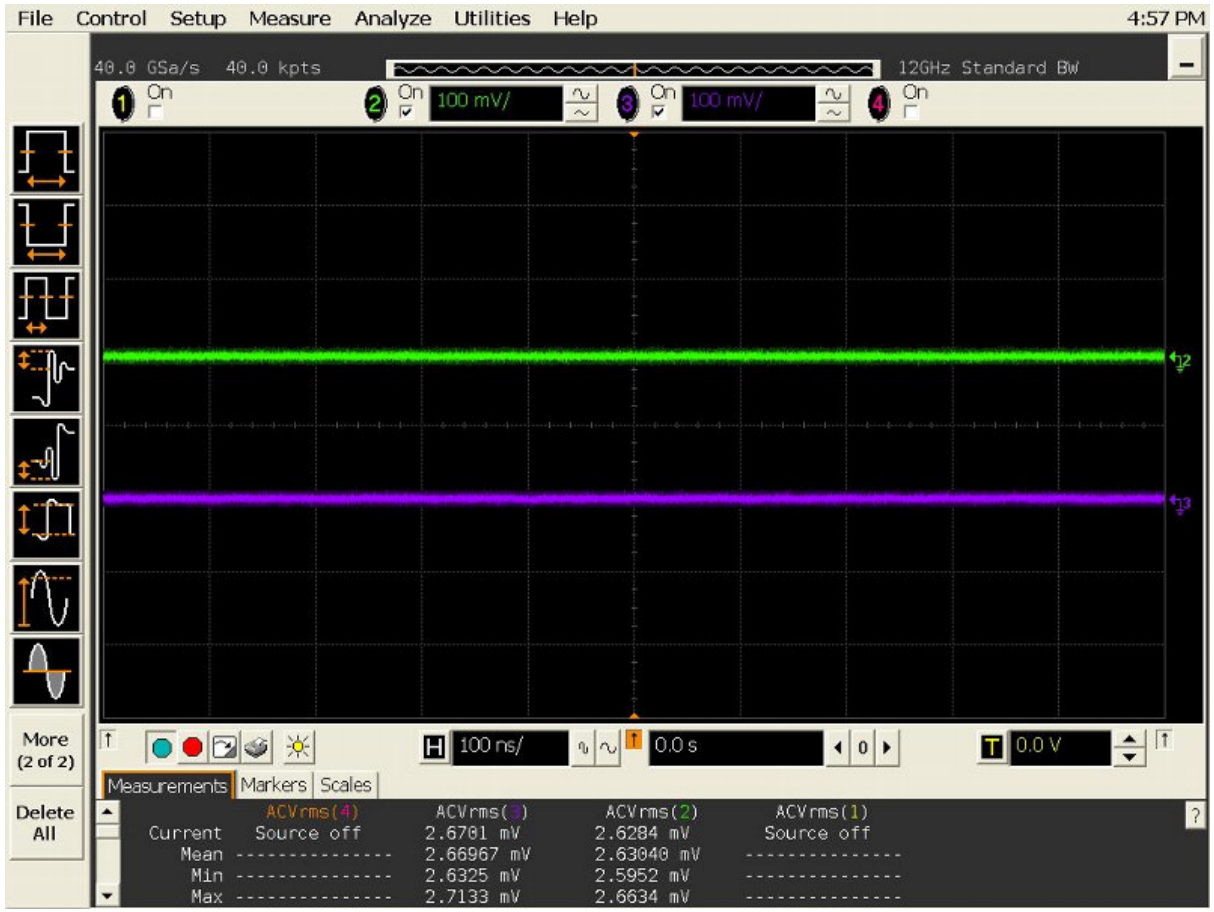
- **Full automation for simple, repeatable testing**
- **Industry leadership and active PHY/LOGO committee participation**
- **Signal Integrity (lowest industry noise floor by 2-2.5 times, better probing)**

Vertical Noise Impact on Amplitude Accuracy

High bandwidth scopes have widely varying degrees of front-end noise, which can lead to significant differences in measurement results regarding amplitude and timing.

Agilent Technologies' DSO81204B 12GHz real-time oscilloscope has nearly half of the noise of the LeCroy SDA11000 and over 60% less noise than the Tektronix DPO70000 at 100mV/div and at all other major vertical sensitivity settings.

Agilent DSO81204B: <3mV RMS noise at 100mV/div vertical sensitivity setting



Agenda

- **Transmitter (TX) Validation**
  - Specification Compliance Testing
  - **Jitter Margin Testing**
  - Eye Diagram Mask Template Testing
  - Bit Failure Analysis
  - Spread Spectrum Clock (SSC) Accuracy Testing
- Receiver (RX) Validation
  - Stressed Eye Diagram Testing
- Full Compliance Test Suite
  - ValiFrame Software: Simplifying Test with Automation

SATA 1.0a and SATA II Jitter Differences

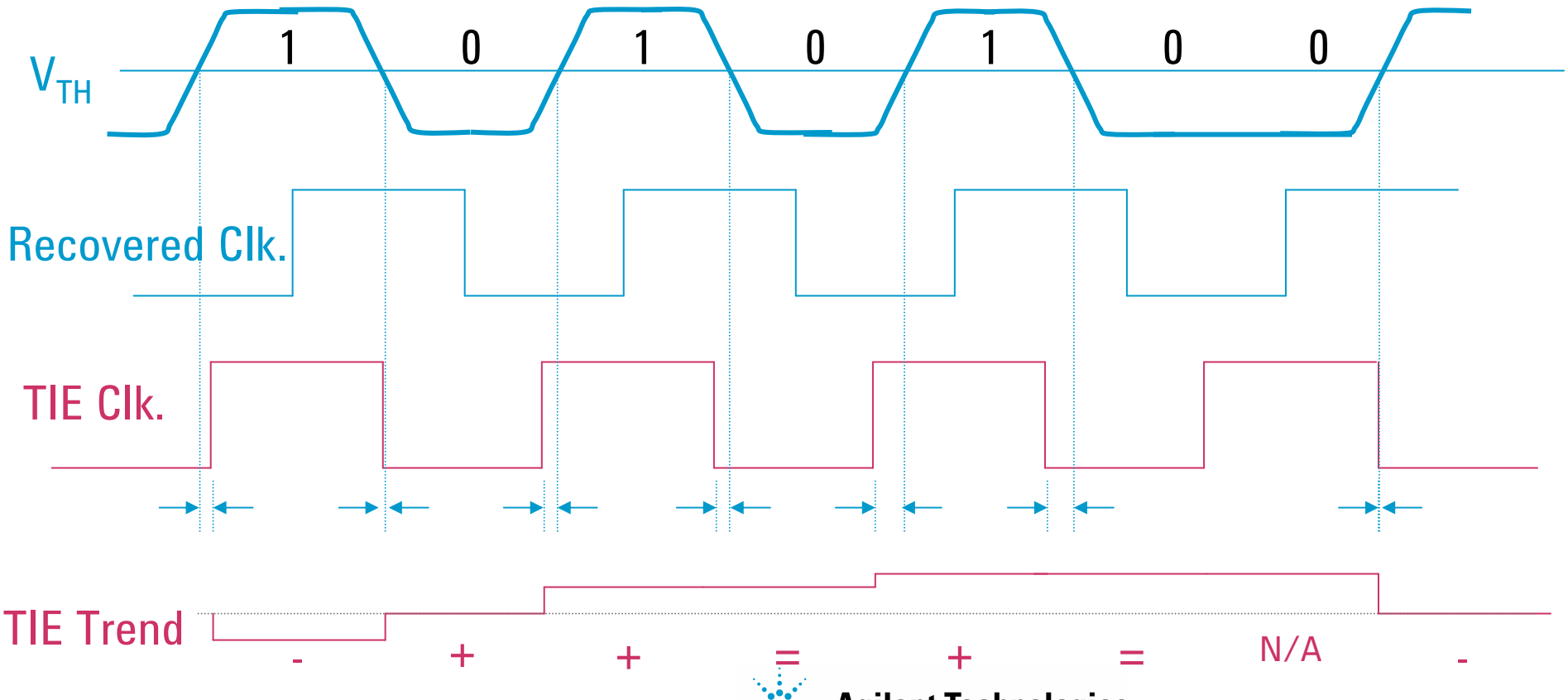
- **SATA II covers both 1.5Gbps and 3.0Gbps data rates and replaces the SATA 1.0a specification**

- **SATA 1.0a used 'Data-to-Data' jitter measurements over 5UI and 250UI**
  - **These are NOT simply *N-Cycle Period Jitter* measurements**
  - **They do not use any clock recovery, as the measurements are made from edge-to-edge**
  - **With the advent of SW PLL clock recovery in scopes, better Time-Interval Error jitter methods exist today**

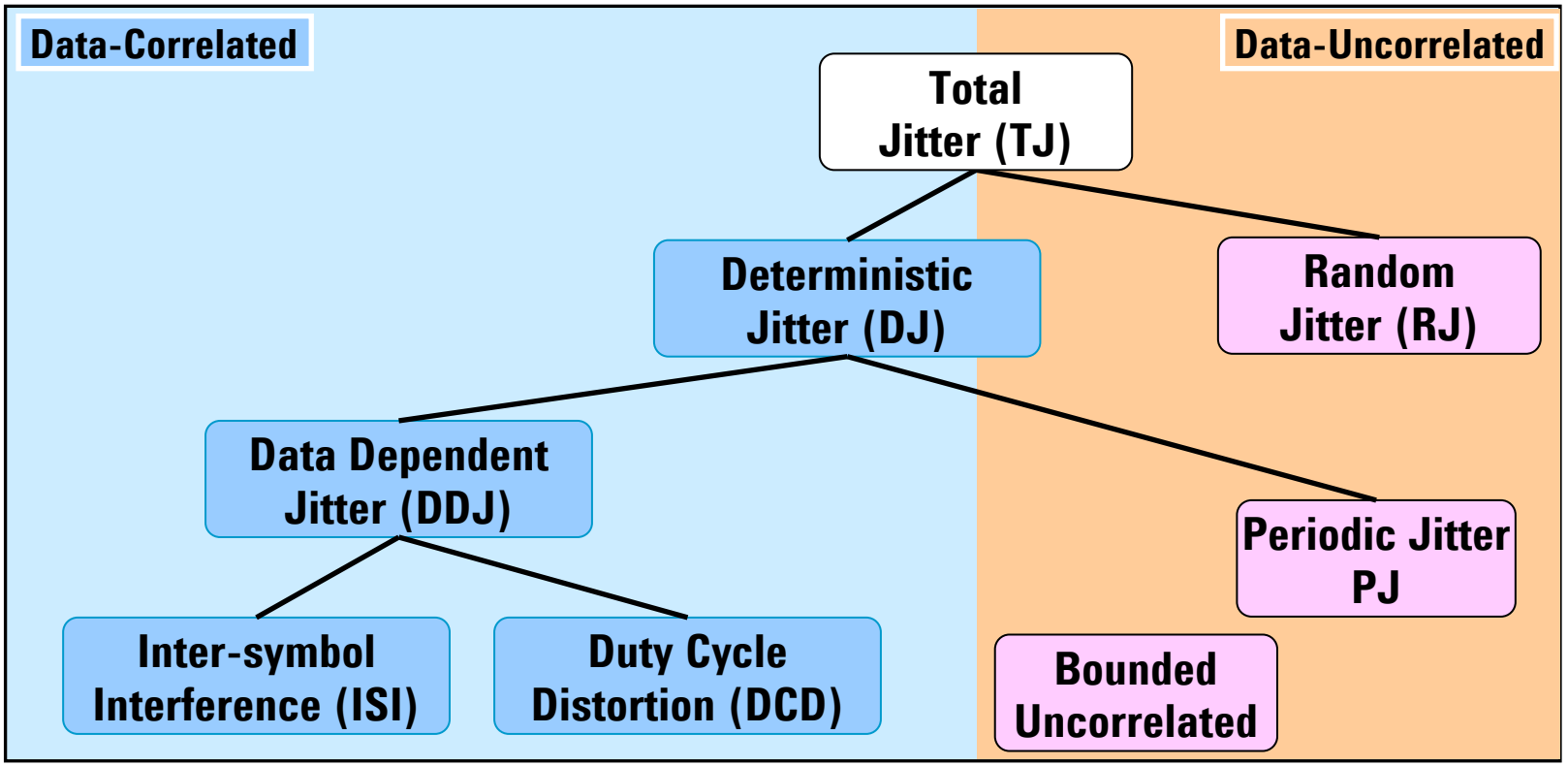
- **NEW!!! SATA II 1.5Gbps & 3.0Gbps jitter measurements are both made using 'Clock-to-Data' methods with 2nd order SW PLL clock-recovery**

Clock-to-Data Jitter: Time Interval Error Trend

A best-fit linear regression of the data transition time-tags is used to recover a fixed frequency (constant phase and frequency) clock, or a SW PLL is used to actively recover the clock from the data transitions.

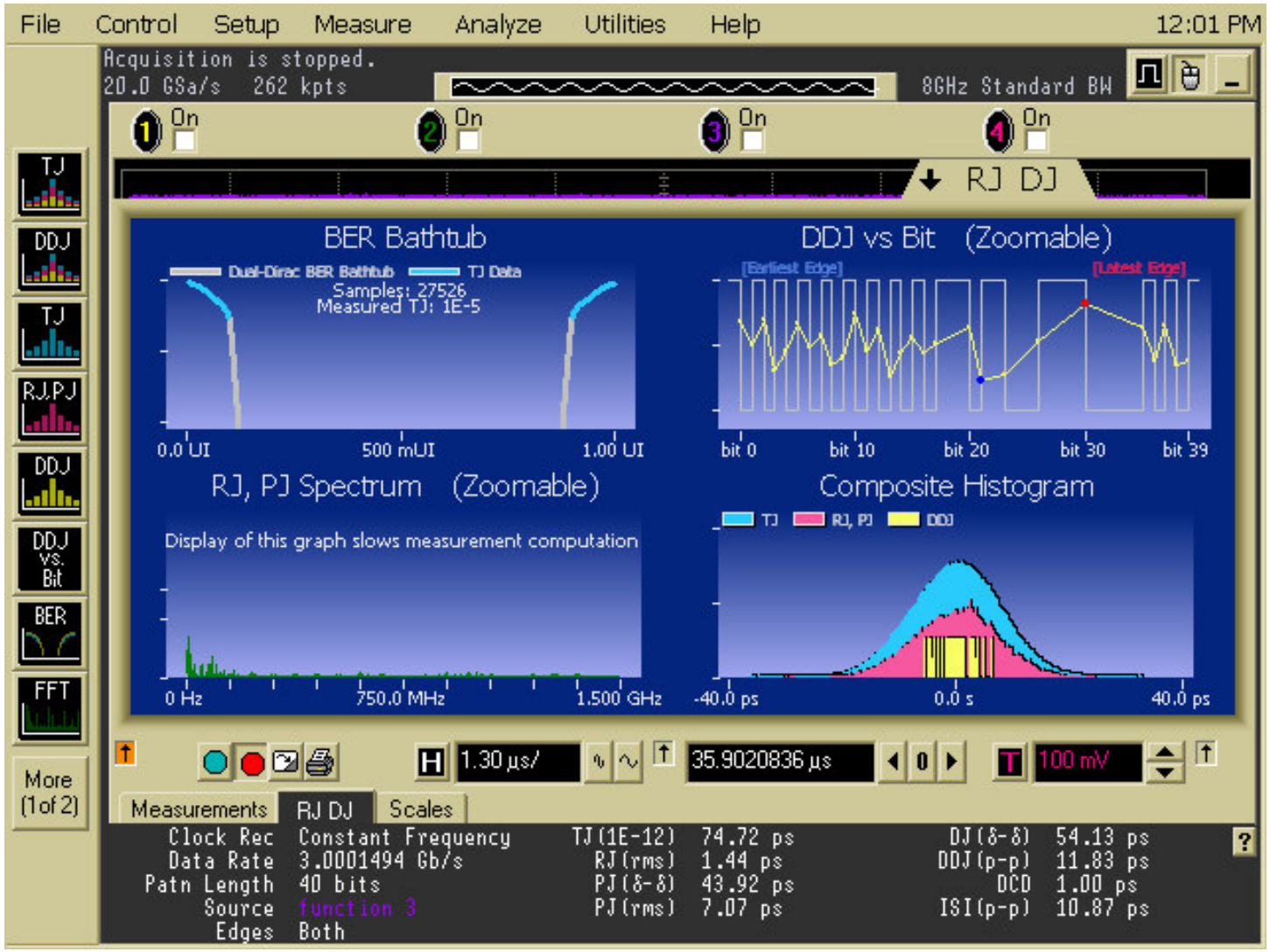


How Jitter is Defined for Digital Systems

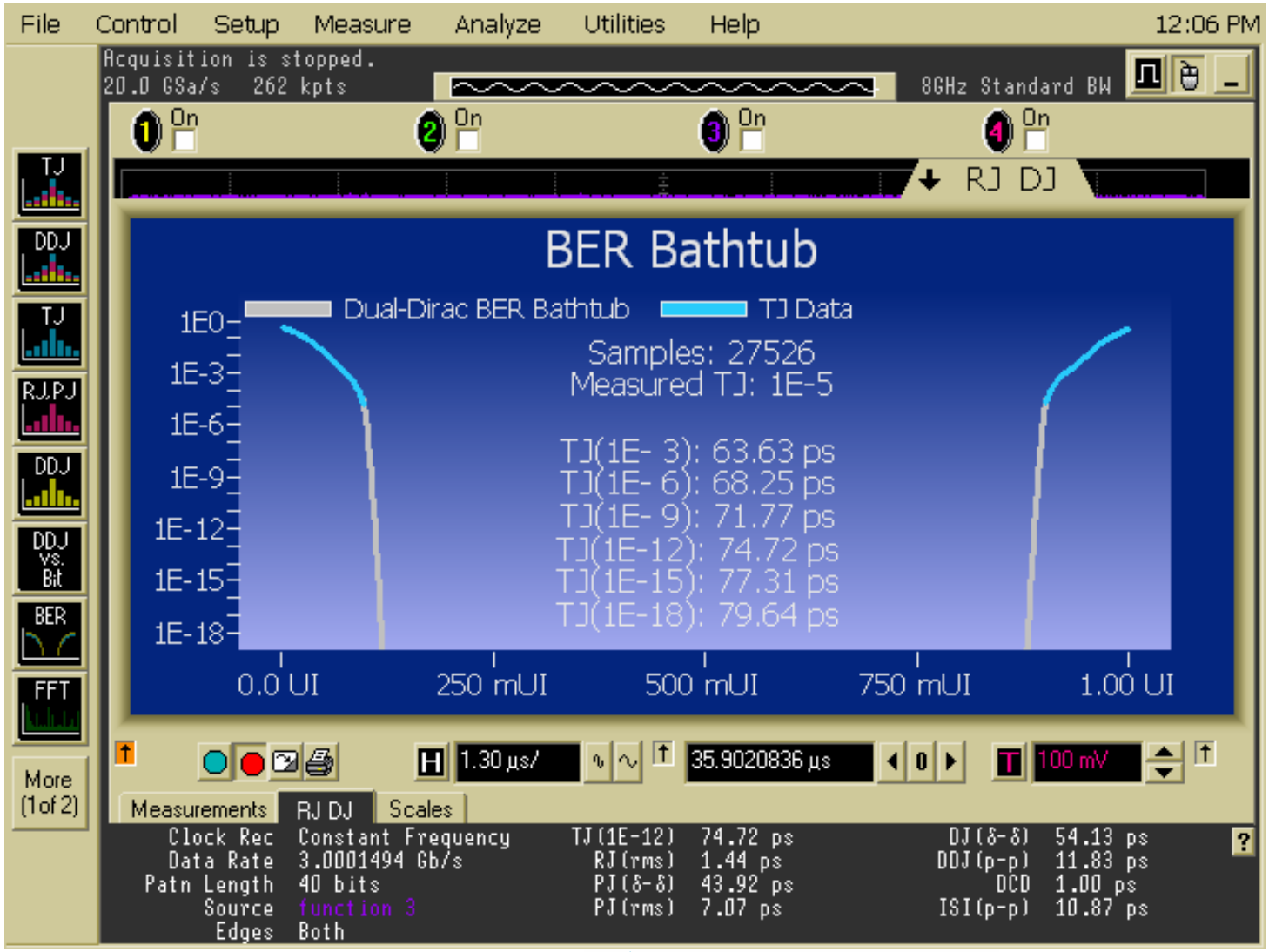


Signal jitter can be composed of several different types from several different mechanisms

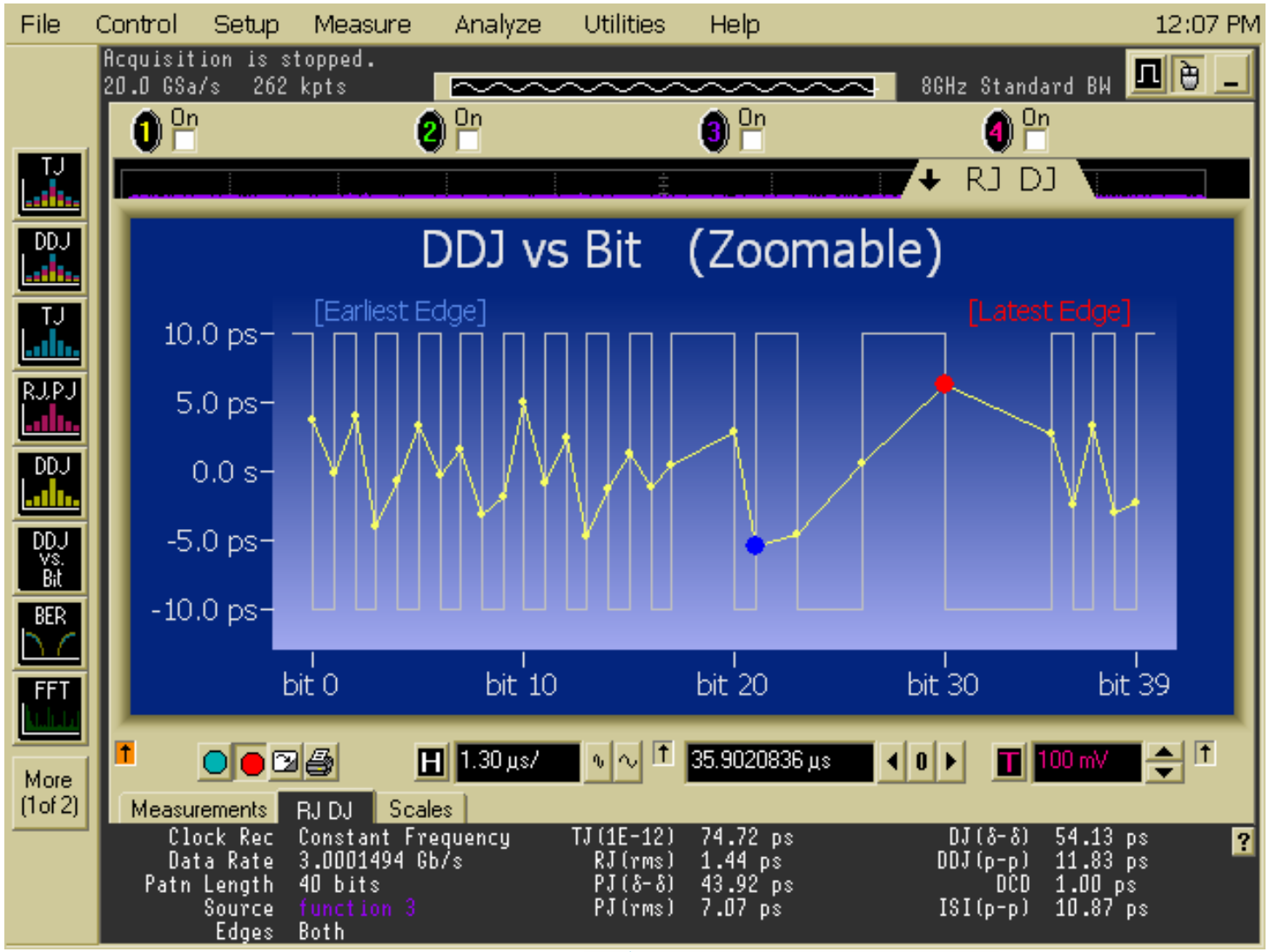
Jitter Analysis and TJ Estimation at 10^{-12} BER



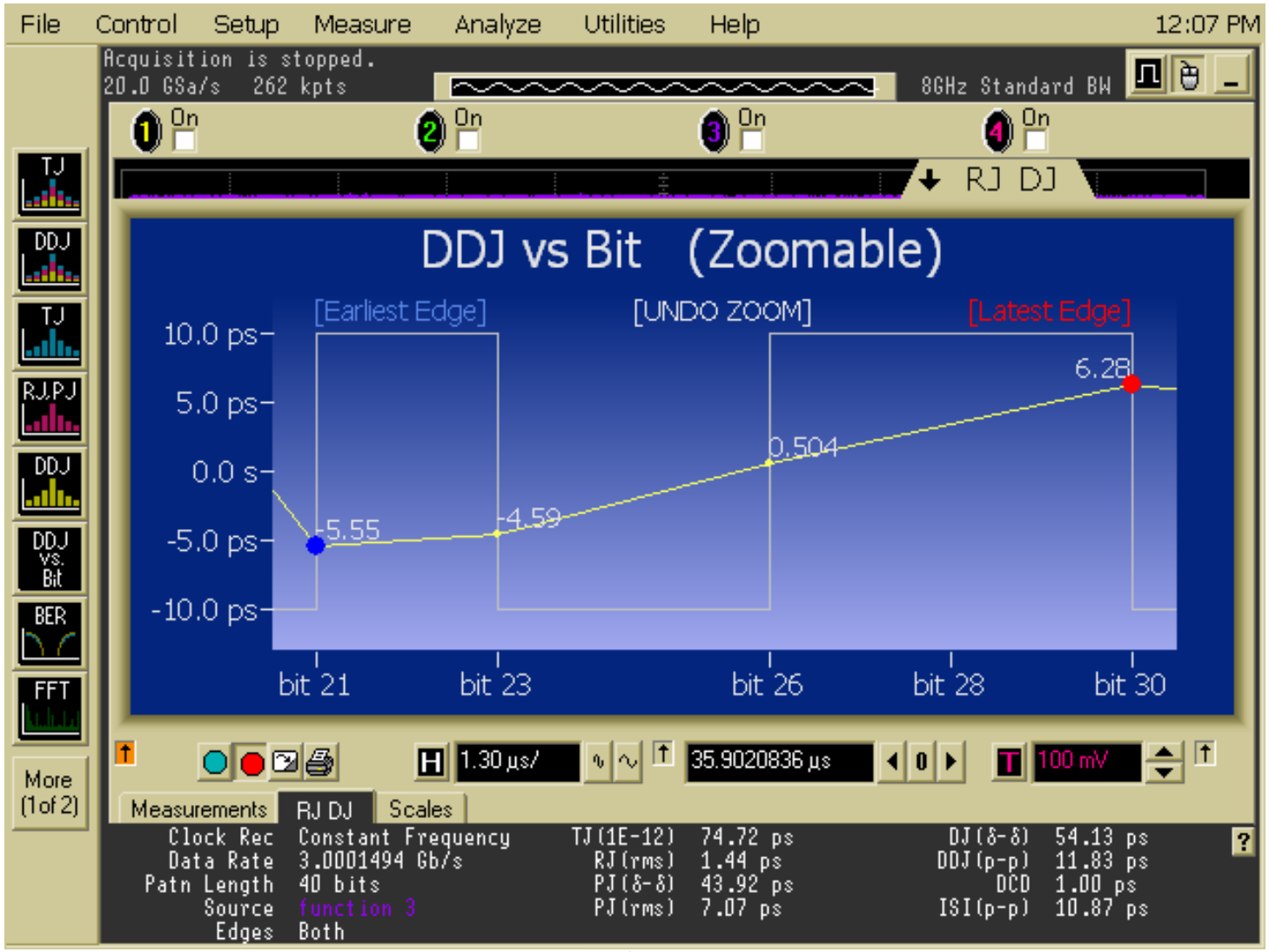
Fast & Accurate TJ Estimation



Quickly Assess Problem Bits or Sequences



Numerical ISI Values Per Transition



Agenda

- **Transmitter (TX) Validation**
  - Specification Compliance Testing
  - Jitter Margin Testing
  - **Eye Diagram Mask Template Testing**
  - Bit Failure Analysis
  - Spread Spectrum Clock (SSC) Accuracy Testing
- Receiver (RX) Validation
  - Stressed Eye Diagram Testing
- Full Compliance Test Suite
  - ValiFrame Software: Simplifying Test with Automation

SATA 1.0a Electrical Mask Templates

These masks are defined in the 1.0a Electrical Specification for quickly testing voltage and jitter margins for 1.5 Gbps Drives and Hosts:

- **1.5 Gbps TX Mask Templates**
  - **Gen1i/m : 5UI and 250UI (2 masks)**
- **1.5 Gbps RX Mask Templates**
  - **Gen1i/m : 5UI and 250UI (2 masks)**

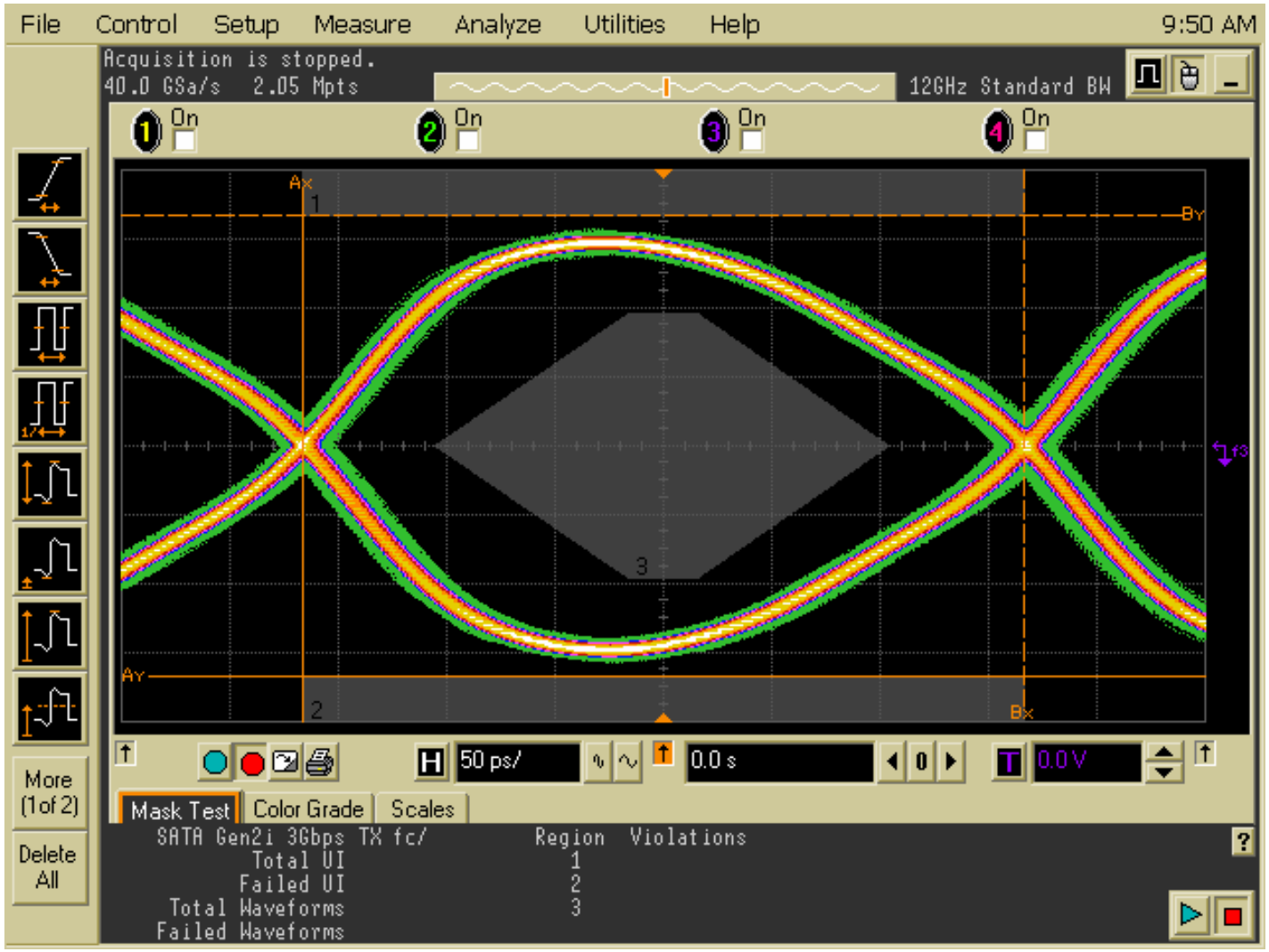
SATA II Electrical Mask Templates

Although not directly defined by the SATA II Electrical Specification, we have created mask templates that implement the recommended 2nd order PLL clock-recovery for quickly testing voltage and jitter margins for 3Gbps Drives and Hosts:

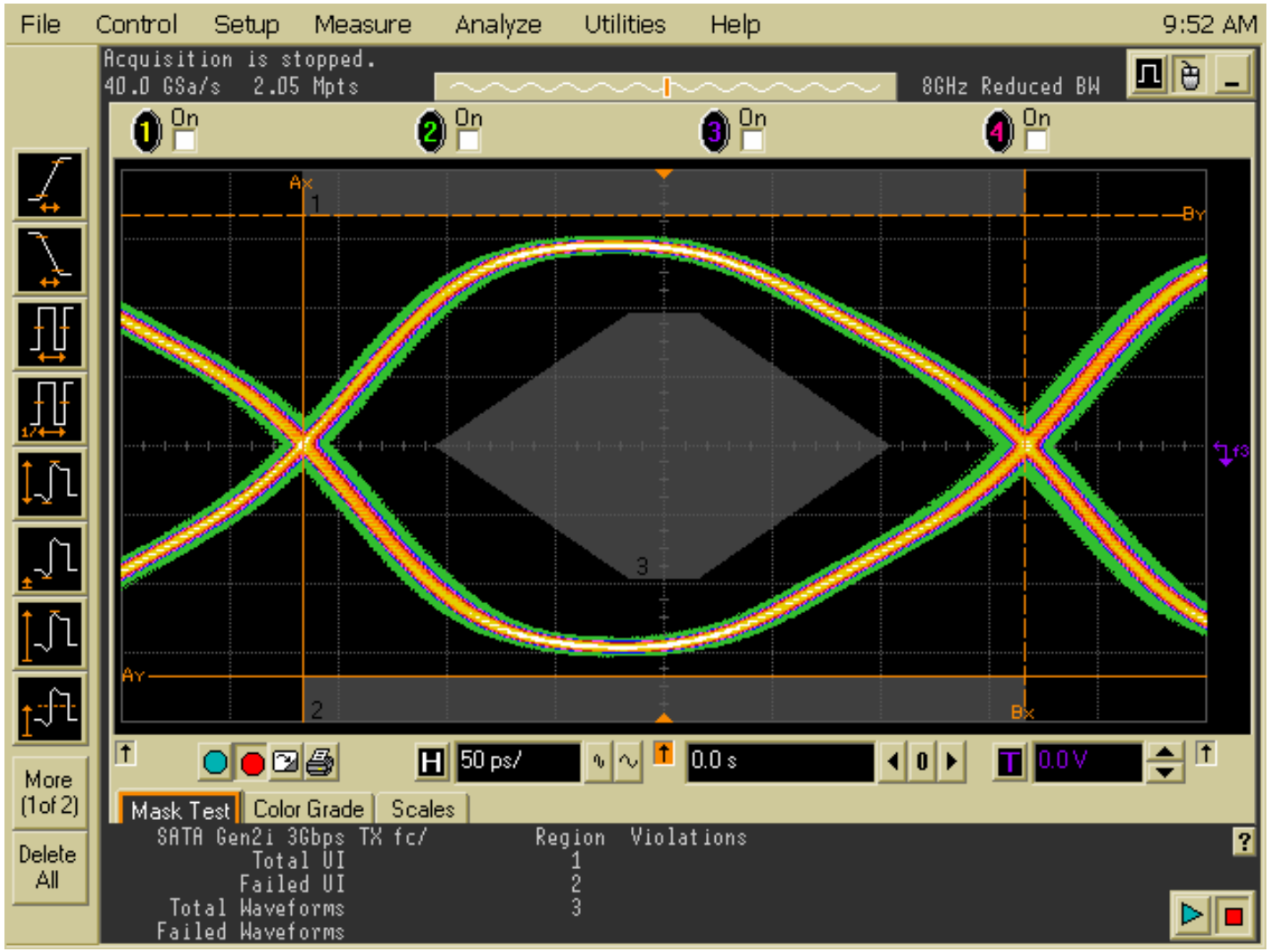
•3.0 Gbps TX/RX Mask Templates

- **Gen2i : $f_{baud}/10$ & $f_{baud}/500$ (2 masks)**
- **Gen2m : $f_{baud}/10$ & $f_{baud}/500$ (2 masks)**
- **Gen2x : $f_{baud}/1667$ (1 mask)**

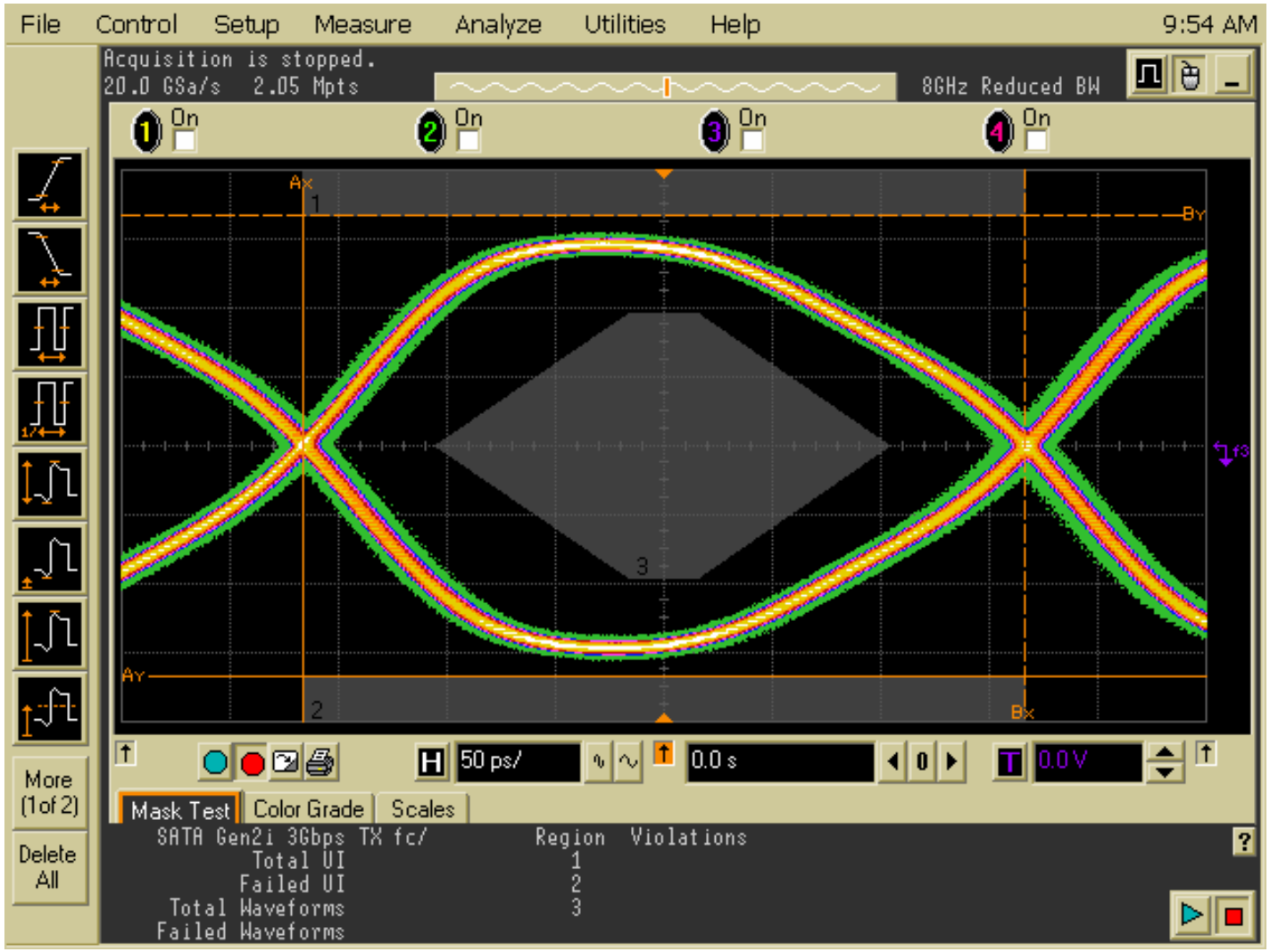
3.0Gbps Eye Diagram at 12GHz and 40GSa/s



3.0Gbps Eye Diagram at 8GHz and 40GSa/s



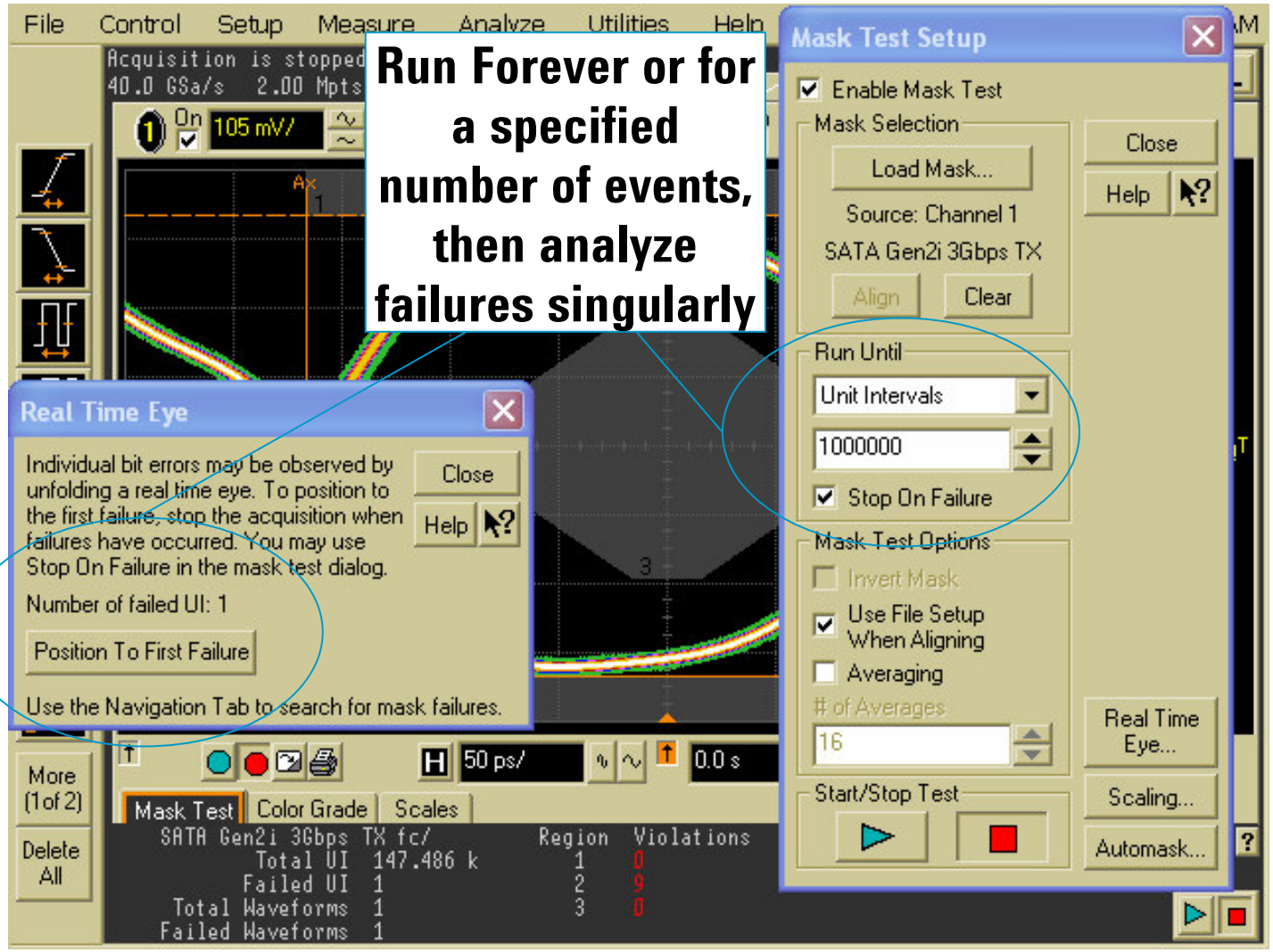
3.0Gbps Eye Diagram at 8GHz and 20GSa/s



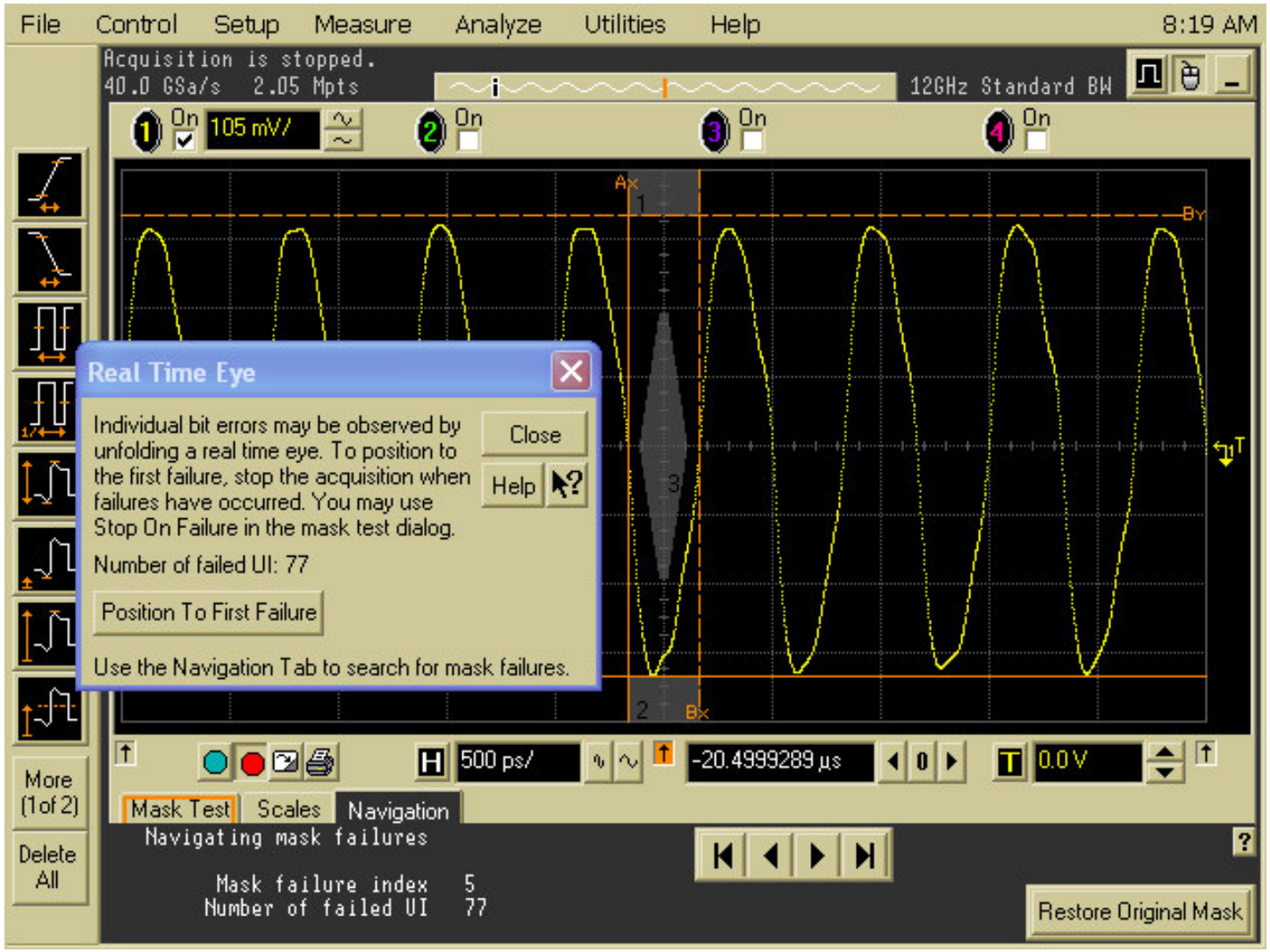
Agenda

- **Transmitter (TX) Validation**
  - Specification Compliance Testing
  - Jitter Margin Testing
  - Eye Diagram Mask Template Testing
  - **Bit Failure Analysis**
  - Spread Spectrum Clock (SSC) Accuracy Testing
- Receiver (RX) Validation
  - Stressed Eye Diagram Testing
- Full Compliance Test Suite
  - ValiFrame Software: Simplifying Test with Automation

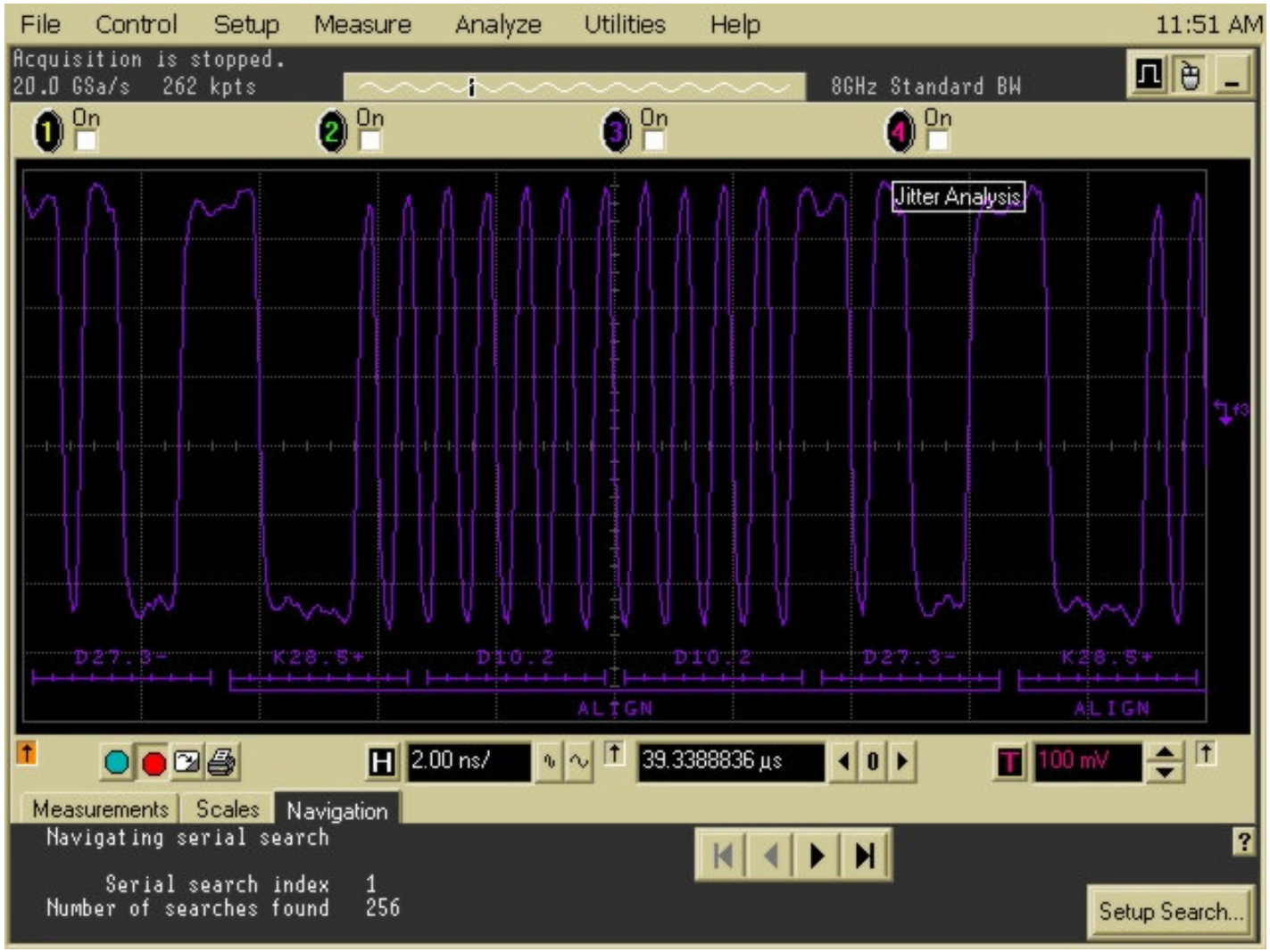
Real Time Eye Analysis With Bit-Failure Unfolding



Real Time Eye Analysis With Bit-Failure Unfolding



8b/10b Decode with Search Can Isolate Failures



Agenda

- **Transmitter (TX) Validation**
  - Specification Compliance Testing
  - Jitter Margin Testing
  - Eye Diagram Mask Template Testing
  - Bit Failure Analysis
  - **Spread Spectrum Clock (SSC) Accuracy Testing**
- Receiver (RX) Validation
  - Stressed Eye Diagram Testing
- Full Compliance Test Suite
  - ValiFrame Software: Simplifying Test with Automation

SSC Definition

Spread spectrum clocking is the intentional downspreading of the transmitter's output data rate in order to reduce the focused transmission power at any 120kHz frequency bandwidth from DC to half the data rate. This is done to allow devices to pass stringent EMI requirements.

Typically, **SSC is implemented by frequency modulating the data output with a 30-33kHz triangular profile** (or Hershey's kiss profile), and the allowed downspread range (modulation deviation) is from the nominal data rate to -0.5% of the nominal data rate. For 3.0Gbps Serial ATA, this range is from 3.0Gbps to 2.985Gbps, or a total of 15MHz downspread from the nominal 3.0Gbps data rate.

SSC Measurement Definition

Spread spectrum clocking is best measured using a measurement trending software, like Agilent's EZJIT product, to trend the unit interval of the signal under test. It is best to use full sample rate to accurately capture the data edge timing events at the receiver sampling threshold (typically zero volts). **With 2.05Mpts of acquisition memory at 40GSa/s, the Agilent DSO80000 Series Infiniium oscilloscopes are fully capable of capturing over 1.5 full cycles of the SSC clock period, which is more than 150,000 cycles of the 3.0Gbps data**. It is recommended to capture and analyze many cycles of the SSC clock over a long period of time (many seconds) to test the SSC performance over a variety of system environmental conditions.

SSC Measurement Best Practices

- **Use a 1010101010 (D10.2) data output pattern, if available; in SATA this is referred to as the High Frequency Test Pattern (HFTP) and is defined in Section 6.1.11**
  - This allows for the maximum number of transitions on the signal under test, and for even spacing between measurements on the data rate trend; it also simplifies the frequency content of the data stream; EZJIT will interpolate through transition gaps in non HFTP patterns, which allows for a linear response of the smoothing filter
- **Adjust the signal display on the oscilloscope so that it occupies as much of the vertical display area as possible without going off screen**
  - This minimizes the vertical noise in the measurement system by maximizing the signal to noise ratio

Measuring the SSC Profile

The bandwidth of the TIE spectrum is limited by:

Data Rate on the high-end

Timebase on the low-end

Since we want to isolate the 30-33kHz SSC modulation frequency and its relevant harmonics, we can:

Use smoothing to low-pass filter out higher frequency jitter sources

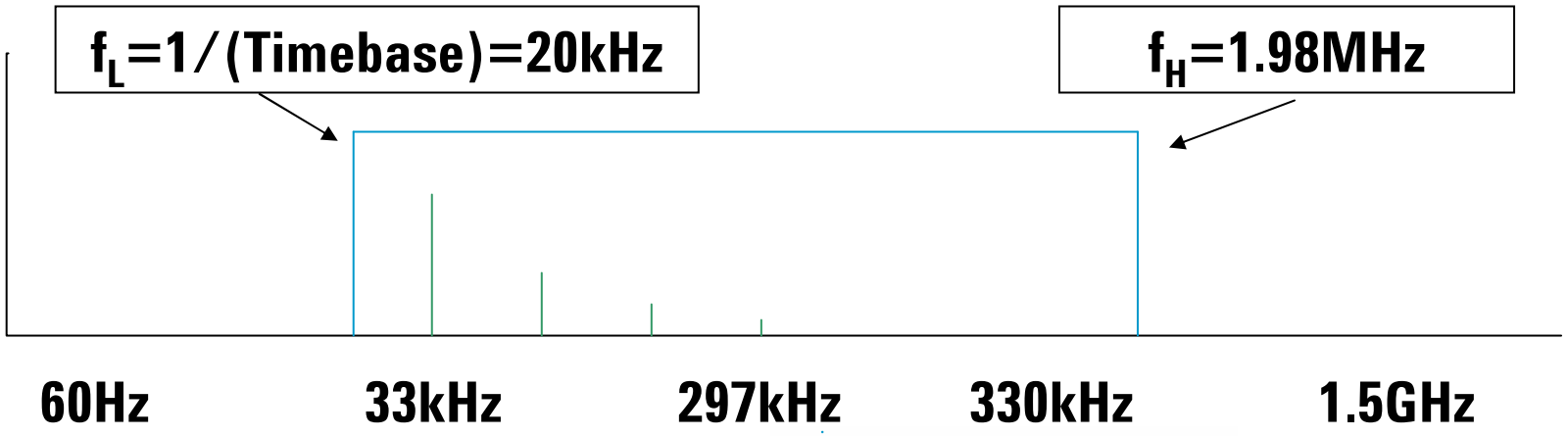
Limit memory depth to high-pass filter out lower frequency jitter sources

Using the Jitter TIE Smoothing Function

The number of smoothing points needed is determined by the low-pass cutoff frequency desired:

$$N_{smooth\text{-}points} = 0.4428 * (Sample\ Rate\ /\ BW_{LPF})$$

Where Sample Rate is the carrier frequency of the data and not the sample rate of the oscilloscope's ADC.



SSC Measurement Best Practices (continued)

•Use the "Smoothing" capability in EZJIT to low pass filter the frequency range of the SSC measurement to the specified 1.98MHz (60 times the 33kHz SSC modulation carrier)

- **See Section 6.4.11 of the Serial ATA II: Electrical Specification 1.0 for more details on the setup of the low-pass filter**
- **The appropriate number of smoothing points can be calculated using the following formula:**

  Nsmooth = 0.4428 * (edge transition rate/desired 3dB cutoff frequency)

  OR

  Nsmooth = 0.4428 * (1.5GHz (for HFTP)/1.98MHz) = 335 points

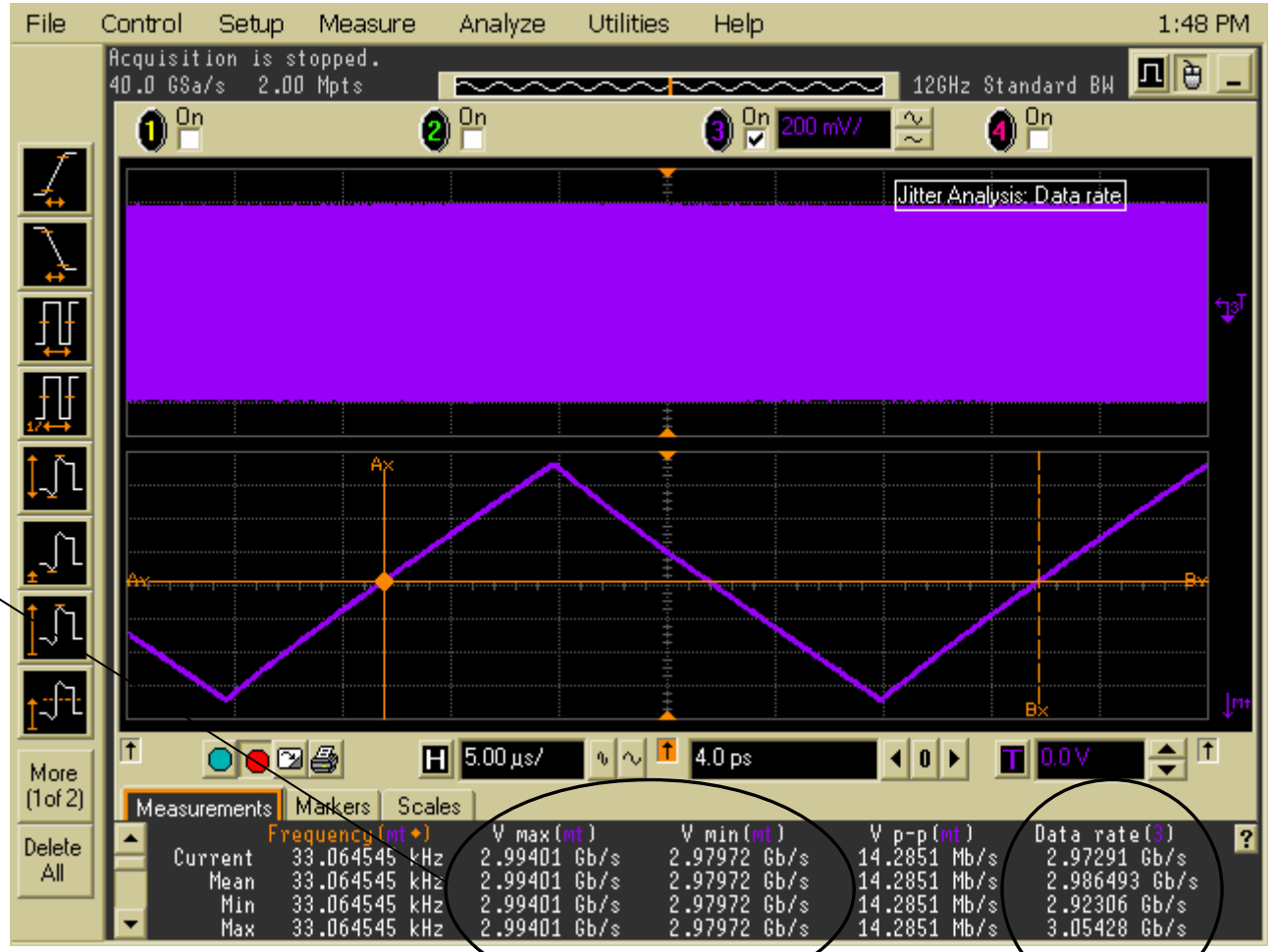
- **Use automated Infiniium measurements to precisely measure SSC modulation frequency and modulation depth automatically, and to collect statistical measurement information over many acquisitions**

Agilent DSO81204B/EZJIT Plus 2Mpts 40GSa/s

Standard Vmax and Vmin measurement quickly measure the Max and Min Data Rate when applied to the filtered measurement trend, per the SATA II specification.

One setup, precise results and statistical trends over many acquisitions.

Observe the unfiltered raw data rate using the standard Data Rate measurement for worst-case conditions on the transmitter.



Summary

•Agilent's EZJIT measurement trending software allows you to quickly analyze and precisely measure your SSC modulation frequency and modulation deviation.

- **Enough memory depth to capture more than a full SSC period**
- **Built-in smoothing of the data rate trend to properly low-pass filter the measurement to 1.98MHz per the specification**
- **Automatic measurements for precision and simplicity**
- **Statistical trends of filtered data rate measurement per the specification**

Agenda

- **Transmitter (TX) Validation**
  - Specification Compliance Testing
  - Jitter Margin Testing
  - Eye Diagram Mask Template Testing
  - Bit Failure Analysis
  - Spread Spectrum Clock (SSC) Accuracy Testing
- **Receiver (RX) Validation**
  - **Stressed Eye Diagram Testing**
- **Full Compliance Test Suite**
  - ValiFrame Software: Simplifying Test with Automation

Receiver Stress Testing

Similar to far-end TX validation tests

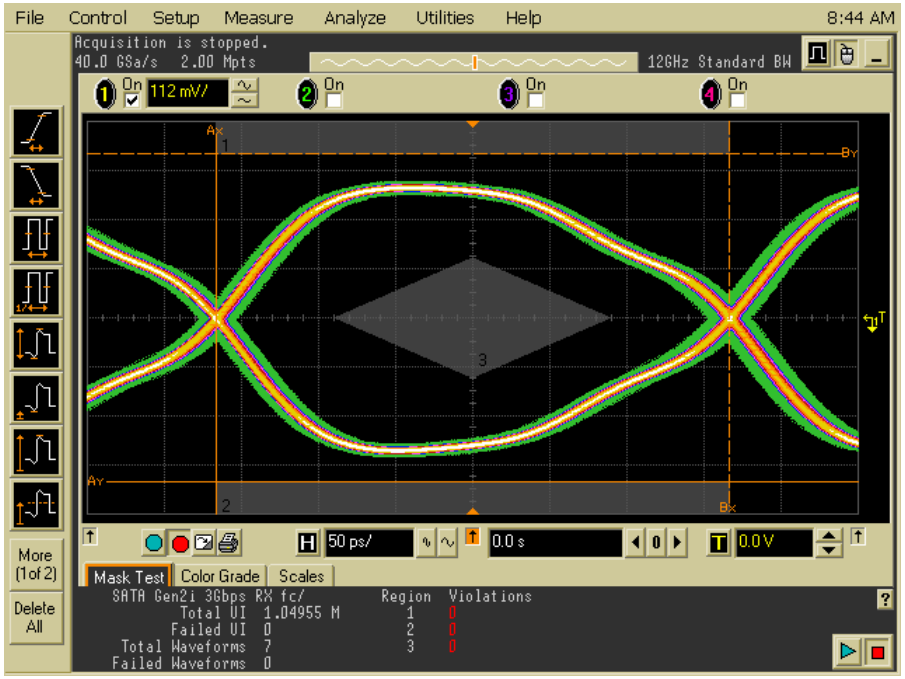
Use stimulus from pulse/pattern generator to create stressed-eyes for RX validation

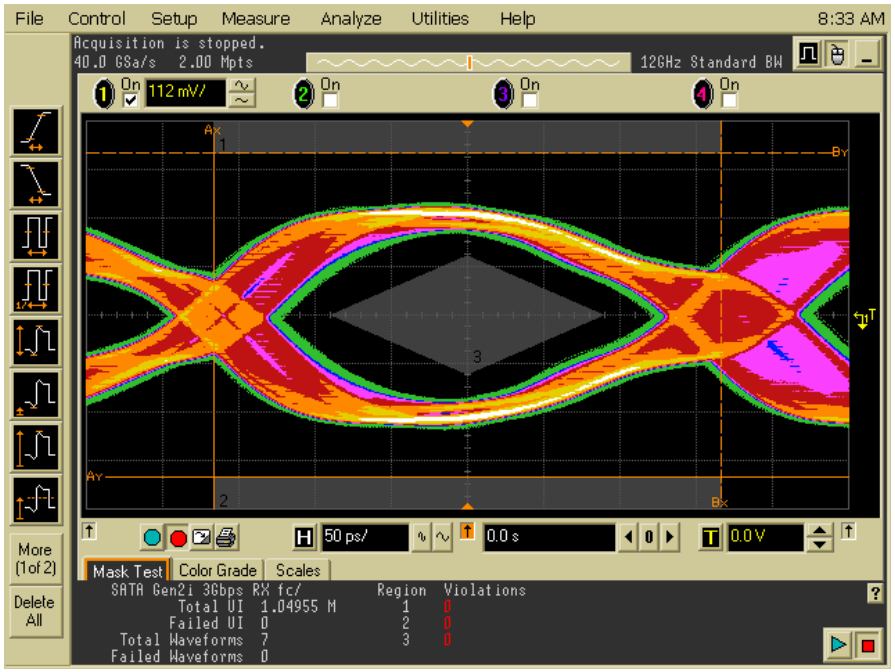
Use oscilloscope RX masks to calibrate jitter and voltage amplitudes of stressed eyes

Identify bit failures as RX or TX signal integrity problem

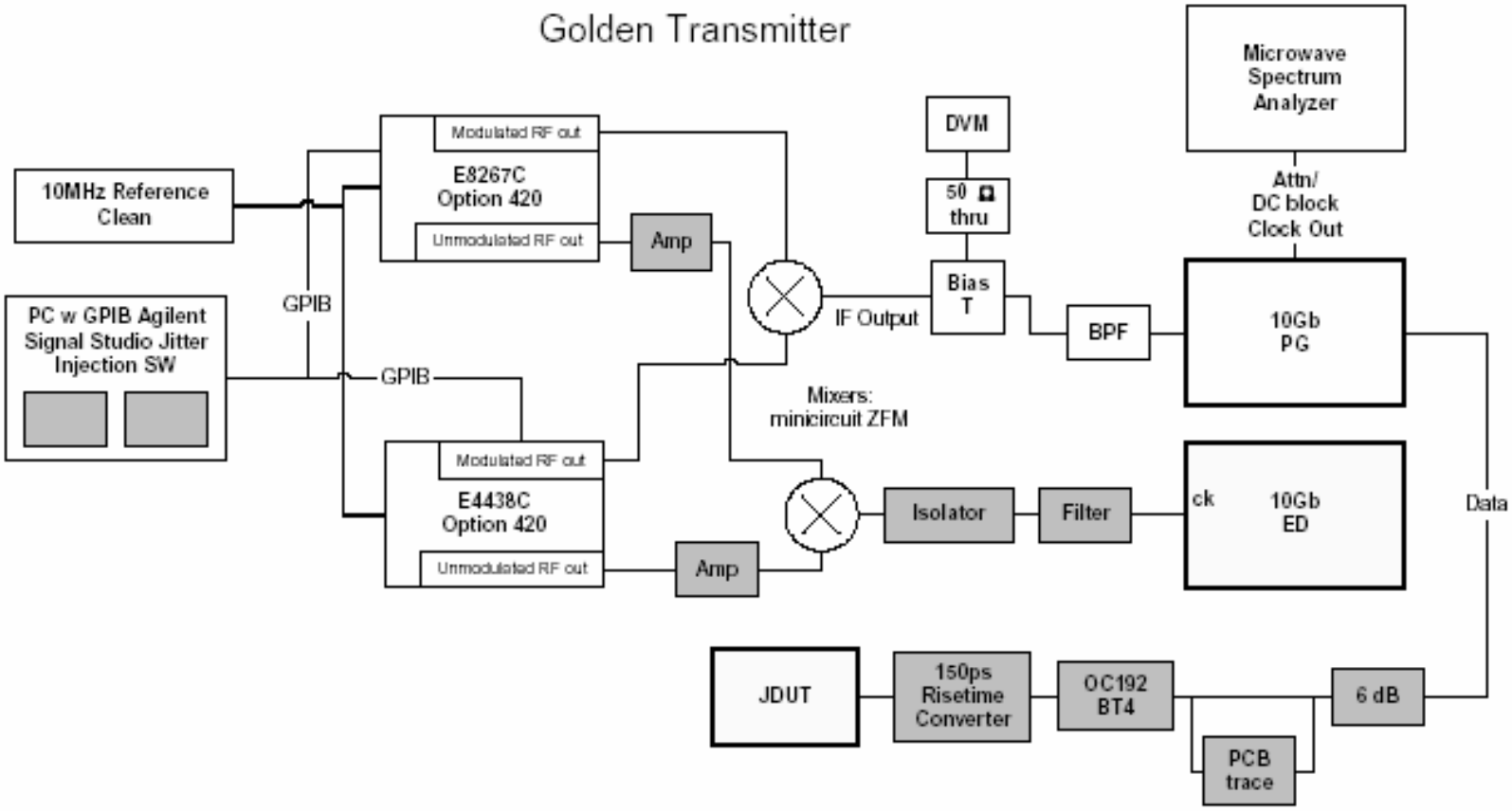
RX Stressed Eye Calibration

Reduce pulse/pattern generator drive amplitudes and use offset, FM/PM inputs and passive in-circuit loss lines to add RJ, DJ, ISI, DCD to stress RX eye against specification

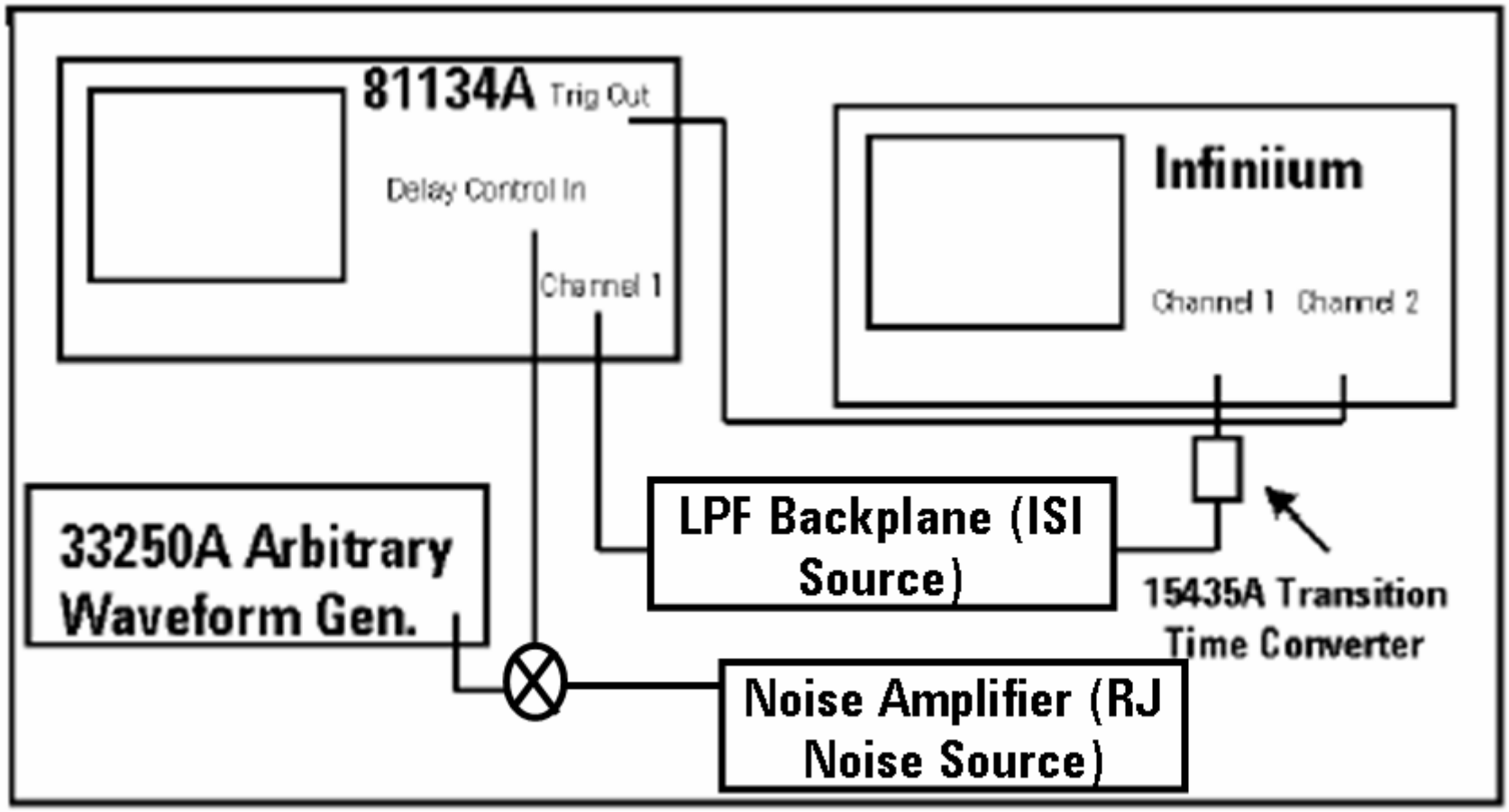




Agilent Precision Jitter Transmitter



Agilent 'Bronze' Jitter Transmitter



Agenda

- **Transmitter (TX) Validation**
  - Specification Compliance Testing
  - Jitter Margin Testing
  - Eye Diagram Mask Template Testing
  - Bit Failure Analysis
  - Spread Spectrum Clock (SSC) Accuracy Testing
- **Receiver (RX) Validation**
  - Stressed Eye Diagram Testing
- **Full Compliance Test Suite**
  - ValiFrame Software: Simplifying Test with Automation

Tests Required for SATA-IO Product Certification

•PHY-TSG-OOB (Transmitter Testing)

•A list of Transmitter test ran with Drive or Host sending a variety of test patterns or responding to Out Of Band signaling. Measurements are performed on an **10GHz oscilloscope** with a **pulse pattern generator** as stimulus

•RXTX (Return Loss)

•A list of return loss test performed on a **DCA** with **TDR module**.

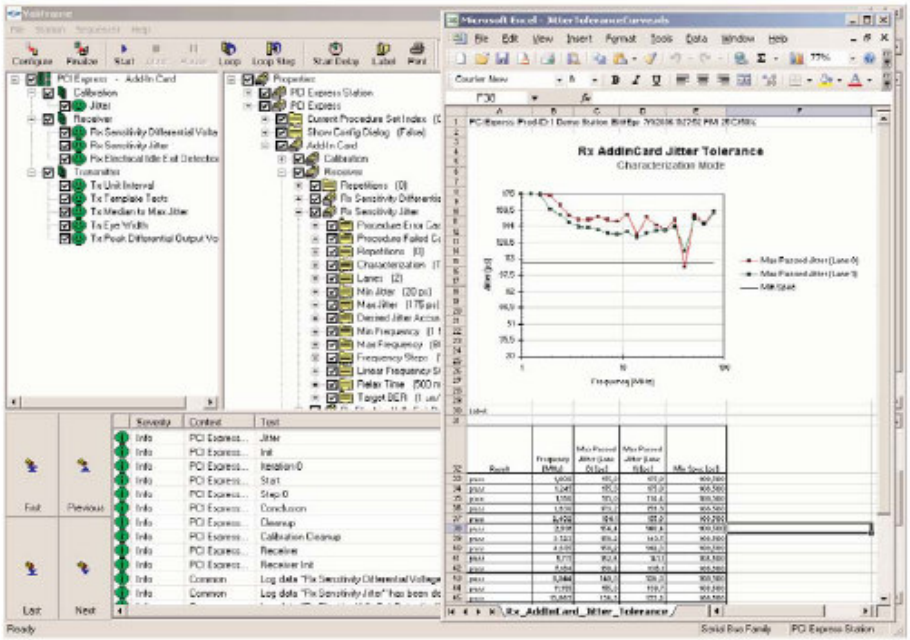
•RSG (Receiver Stress Testing)

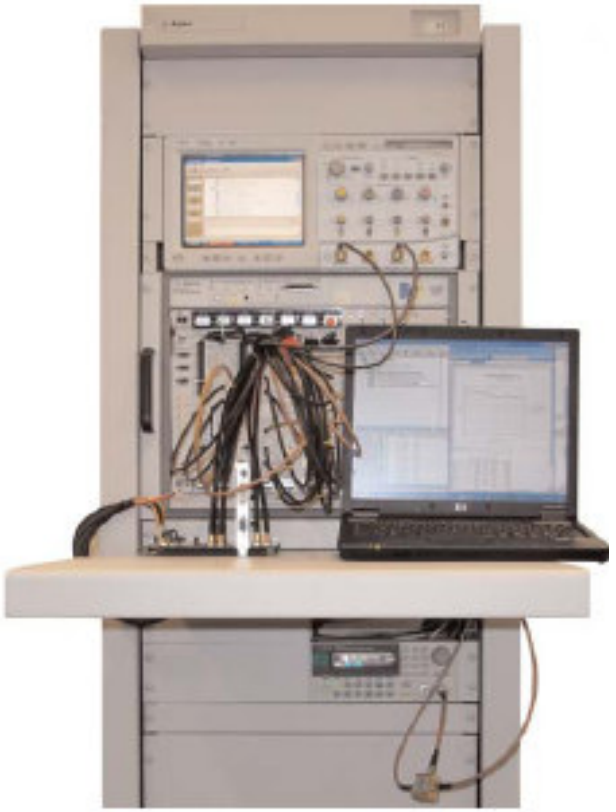
•A list of Receiver stress tests ran with the Drive or Host in Far End Retimed Loopback mode. Measurements are performed on a o**scilloscope** with a **pulse pattern generator** injecting controlled amounts of jitter.

Agenda

- **Transmitter (TX) Validation**
  - Specification Compliance Testing
  - Jitter Margin Testing
  - Eye Diagram Mask Template Testing
  - Bit Failure Analysis
  - Spread Spectrum Clock (SSC) Accuracy Testing
- **Receiver (RX) Validation**
  - Stressed Eye Diagram Testing
- **Full Compliance Test Suite**
  - **ValiFrame Software: Simplifying Testing with Automation**

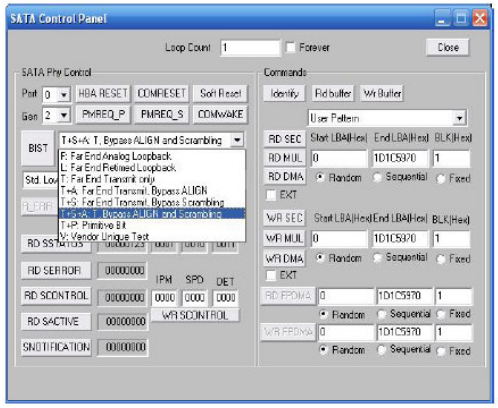
ValiFrame Software from BitifEye www.bitifeye.com





- Uniting all instruments and software seamlessly with **one user interface!**
- **Automating** the all tests required for certification to make testing simple and repeatable!
- Allow for **additional control** of other instruments for non-required testing and debug.

ValiFrame Control Includes the Following



Equipment for Required Testing:

DSO 80000 Real-time Scope

86100 DCA

8113x Pulse Generators

ULINK DriveMaster software

Additional Instrument Control:

Logic Analyzer

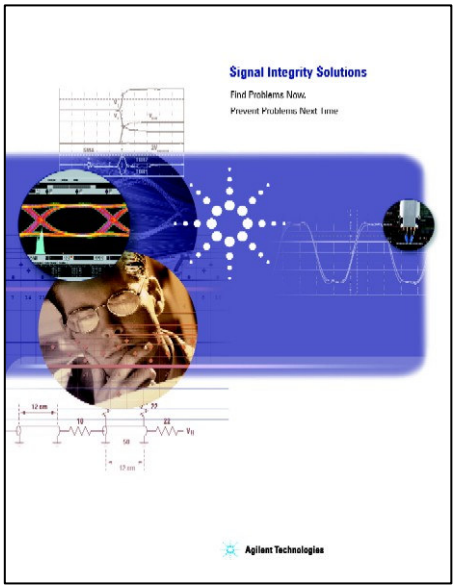
VNA

JBERT

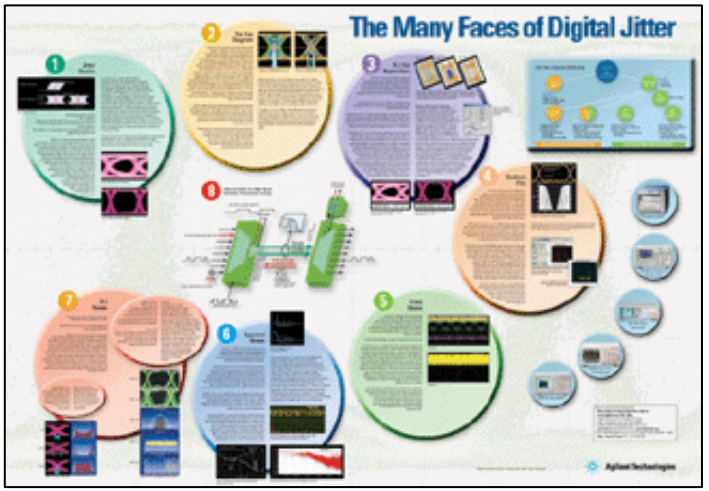
Additional Product Feature:

Control for additional instruments and software can easily be added

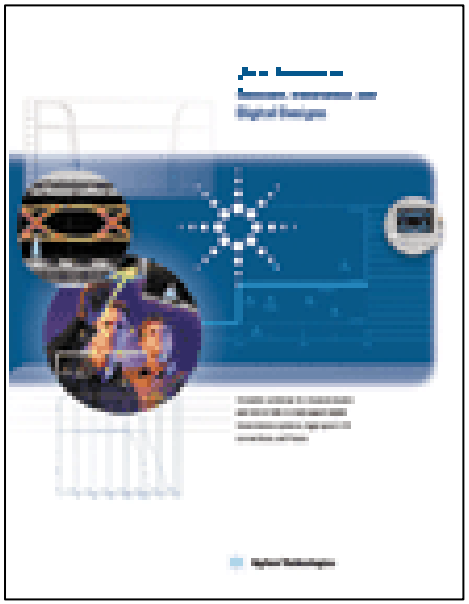
Signal Integrity/Jitter Resources



5988-5405EN

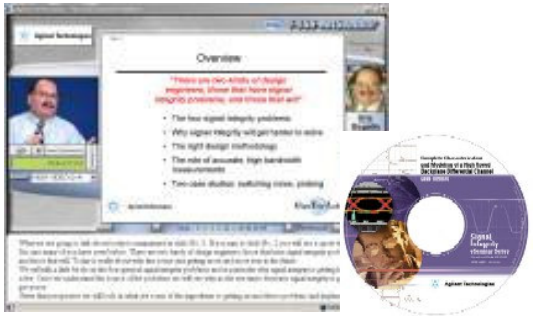


5989-0830EN



5988-9592EN

5988-6915EN



eSeminars
(all available on CD)

5988-9350EN

Product Web Resources

MSO
www.agilent.com/find/mso

DSO80000 Scope/InfiniMax
www.agilent.com/find/infiniimax2

86100 DCA-J
www.agilent.com/find/dca

Jitter Products
www.agilent.com/find/jitter

Logic Analyzer Solutions
www.agilent.com/find/logic

FPGA Active Probe
www.agilent.com/find/fpga

PLTS
www.agilent.com/find/plts

BERTs
www.agilent.com/find/bert

Pulse Generators
www.agilent.com/find/81134a

E2960 Protocol Tools
www.agilent.com/find/e2960_series

Application Web Resources

Signal Integrity Application Central
www.agilent.com/find/si

Signal Integrity Series eSeminars
www.agilent.com/find/sigint

Jitter Applications Home page
www.agilent.com/find/jitter_info

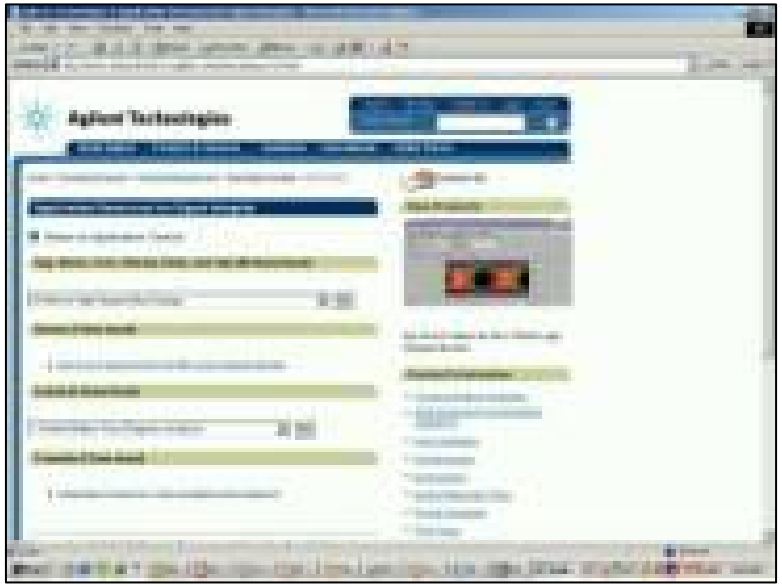
FPGA Debug Application Central
www.agilent.com/find/fpga_debug

PCI Express Application Central
www.agilent.com/find/pci_express

FB-DIMM Application Central
www.agilent.com/find/fb-dimm

Serial Interconnect App. Info
www.agilent.com/find/serial_info

Digital Discussion Forums
www.agilent.com/find/forums



Discussion